ANNA UNIVERSITY: : CHENNAI
UNIVERSITY DEPARTMENTS
REGULATIONS 2019
M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
CHOICE BASED CREDIT SYSTEM

VISION OF DEPARTMENT OF ELECTRONICS ENGINEERING

The Department of Electronics Engineering is committed to produce globally competitive and socially sensitized graduates in Electronics & Communication Engineering. We seek to instill the spirit of creativity and leadership skills enabling the students to make a global impact towards the availability of technology to mankind from all walks of life.

MISSION OF DEPARTMENT OF ELECTRONICS ENGINEERING

- To impart high quality technical education to students from socially and economically diverse backgrounds
- Give solid foundation on Mathematical skills and allied fields of Electronics & Communication
- To produce students with technical competence to design sophisticated systems in Electronics & Communication
- To make high quality research contribution in the field of Electronics, Communication, Networking , VLSI & Signal Processing
- To collaborate with industries in Electronics & Communication in the indigenous product development
- To inculcate qualities of leadership and entrepreneurship in students
- To facilitate adequate exposure to the faculty enabling them to be synchronized with the Cutting edge technology

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UNIVERSITY DEPARTMENTS
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1. PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

I. Enrich students to excel in research leading to cutting edge technology in VLSI design and Embedded Systems and creating competent, innovative, and productive professionals in this field.

II. Provide students with a solid foundation in MOS devices, digital electronics design, analog system design and computer architecture principles leading to VLSI design.

III. Understand the various applications and employ Embedded Systems based solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products for real life problems.

IV. Provide dynamic diverse academic environment to the students and aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and lifelong learning needed for a successful professional career.

V. Inculcate entrepreneurial skills to start industries related to VLSI design and embedded system technologies.

2. PROGRAMME OUTCOMES (POs):

PO#	Graduate Attribute	Programme Outcome
1.	Research aptitude	An ability to independently carry out research /investigation and development work to solve practical problems.
2.	Technical documentation	An ability to write and present a substantial technical report/document
3.	Technical competence	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
4.	Engineering Design	Ability to design and conduct experiments, perform analysis, applying the knowledge of computing, mathematics, science and electronic engineering for designing VLSI and Embedded Systems.
5.	Conduct investigations of complex problems	Interpret the problems of VLSI and Embedded Systems and investigate solutions and work towards improved solutions.
6.	Life-long Learning	Continuously update knowledge with modern tools and technical developments and ensure professional development.

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3. ROGRAMME SPECIFIC OUTCOMES (PSOs):

By the completion of VLSI Design and Embedded Systems programme, students will have the following programme specific outcomes

I. Foundation of VLSI systems: Ability to understand the fundamentals of VLSI systems. Students can assess the basic components and modules of VLSI systems.

II. Foundation of Embedded Systems: Ability to understand the basic principles of Embedded Systems. Students can assess the basic components and modules of Embedded Systems.

III. Foundation of Mathematical concepts: Ability to apply mathematical knowledge to solve complex computations related to the field of VLSI and Embedded Systems.

IV. Applications of VLSI Design and Research ability: Ability to use knowledge in various domains to identify research gaps and hence provide solutions with innovation.

V. Identify the research gaps and provide innovative solutions.

4. PEO/PO Mapping:

PEO	PO					
	PO1	PO2	PO3	PO4	PO5	PO6
I.			✓	✓	✓	
II.	✓					
III.		✓	✓	✓	✓	**7.**
IV.	✓	✓	✓		✓	✓
V.		✓	✓	✓	✓	

L – Low, M – Medium, H - High

Year	Sem	Courses	Program Outcomes					
			PO01	PO02	PO03	PO04	PO05	PO06
First	I	Advanced Applied Mathematics	L		H	H	L	L
		Digital Integrated Circuit Design	H	M	H	H	H	H
		VLSI Architectures for System Design	H	M	H	H	H	H
		Advanced Embedded System Design	H	M	H	H	H	H
		Real Time Embedded System Design	L	M	H	H	L	H
		Research Methodology and IPR	H	H				H
		Audit Course- I						
		Digital System Design Lab	H	H	H	H	H	H
		Embedded Systems Lab	H	H	H	H	H	H
	II	Design for Testability	H	H	H	H	H	H
		CMOS analog IC Design	H	M	H	H	H	H
		Hardware-Software Co-design of Embedded system	H	M	H	H	H	H
		Embedded Automation	H	M	H	H	H	H
		Program Elective Course - I						
		Audit Course - II						
		Analog System Design Lab	H	H	H	H	H	H
		Embedded Automation Lab	H	H	H	H	H	H
		Mini Project with Seminar	H	H	H	H	H	H
Second	III	Program Elective Course – II						
		Program Elective Course – III						
		Program Elective Course – IV						
		Open Elective						
		Dissertation - I	H	H	H	H	H	H
	IV	Dissertation - II	H	H	H	H	H	H

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S. No.	Program Elective Courses	Program Outcomes					
		PO01	PO02	PO03	PO04	PO05	PO06
1.	Solid State Device Modeling	H	M	H	H	H	H
2.	VLSI Signal Processing Techniques	H	M	H	H	H	H
3.	VLSI For Wireless Communication	H	M	H	H	H	H
4.	Low Power VLSI Design	H	M	H	H	H	H
5.	ASIC Design	H	M	H	H	H	H
6.	SoC Design for Embedded System	H	M	H	H	H	H
7.	Network on Chip Design	H	M	H	H	H	H
8.	Advanced CMOS Analog IC Design	H	M	H	H	H	H
9.	Reconfigurable Architectures and Applications	H	M	H	H	H	H
10.	Computer Aided Design for VLSI Systems	H	M	H	H	H	H
11.	Digital Signal Processors and Architectures	H	M	H	H	H	H
12.	Multi-Core Architectures and Programming	H	M	H	H	H	H
13.	Image Analysis and Computer Vision	H	M	H	H	H	H
14.	Quantum Computing	H	M	H	H	H	H
15.	Adaptive Signal Processing Techniques	H	M	H	H	H	H
16.	Pattern Recognition and Machine Learning	H	M	H	H	H	H
17.	Distributed Embedded Computing	H	M	H	H	H	H
18.	Embedded Networking	H	M	H	H	H	H
19.	Real Time Operating Systems	H	M	H	H	H	H
20.	Embedded C Programming	H	M	H	H	H	H
21.	Embedded Automotive Systems	H	M	H	H	H	H
22.	MEMS and Microsystems	H	M	H	H	H	H
23.	RF IC Design	H	M	H	H	H	H
24.	Computational Intelligence	H	M	H	H	H	H
25.	Robotics	H	M	H	H	H	H

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M.E. VLSI DESIGN AND EMBEDDED SYSTEMS
REGULATIONS 2019
I – IV SEMESTER CURRICULA AND SYLLABI

SEMESTER – I

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	MA5159	Advanced Applied Mathematics	FC	3	1	0	4	4
2.	VE5101	Digital Integrated Circuit Design	PCC	3	0	0	3	3
3.	VE5102	VLSI Architectures for System Design	PCC	3	0	0	3	3
4.	VE5103	Advanced Embedded System Design	PCC	3	0	0	3	3
5.	VE5104	Real Time Embedded System Design	PCC	3	0	0	3	3
6.	RM5151	Research Methodology and IPR	RMC	2	0	0	2	2
7.		Audit Course- I*	AC	2	0	0	2	0
PRACTICALS								
8.	VE5111	Digital System Design Lab	PCC	0	0	4	4	2
9.	VE5112	Embedded Systems Lab	PCC	0	0	4	4	2
			TOTAL	**19**	**1**	**8**	**28**	**22**

***Audit Course is Optional

SEMESTER – II

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VE5201	Design for Testability	PCC	3	0	0	3	3
2.	VE5251	CMOS Analog IC Design	PCC	3	0	0	3	3
3.	VE5202	Hardware-Software Co-design of Embedded system	PCC	3	0	0	3	3
4.	VE5203	Embedded Automation	PCC	3	0	0	3	3
5.		Program Elective I	PEC	3	0	0	3	3
6.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
7.	VE5211	Analog System Design Lab	PCC	0	0	4	4	2
8.	VE5212	Embedded Automation Lab	PCC	0	0	4	4	2
9.	VE5213	Mini Project with Seminar	EEC	0	0	4	4	2
			TOTAL	**17**	**0**	**12**	**29**	**21**

***Audit Course is Optional**

SEMESTER – III

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Program Elective II	PEC	3	0	0	3	3
2.		Program Elective III	PEC	3	0	0	3	3
3.		Program Elective IV	PEC	3	0	0	3	3
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	VE5311	Dissertation- I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**12**	**24**	**18**

SEMESTER – IV

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICAL								
1.	VE5411	Dissertation - II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 73

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REGULATIONS 2019
I TO VI SEMESTERS CURRICULA AND SYLLABI (PART – TIME)

SEMESTER – I

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	MA5159	Advanced Applied Mathematics	FC	3	1	0	4	4
2.	VE5101	Digital Integrated Circuit Design	PCC	3	0	0	3	3
3.	VE5103	Advanced Embedded System Design	PCC	3	0	0	3	3
4.		Audit Course- I*	AC	2	0	0	2	0
PRACTICALS								
5.	VE5111	Digital System Design Lab	PCC	0	0	4	4	2
			TOTAL	**11**	**1**	**4**	**16**	**12**

***Audit Course is Optional

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SEMESTER – II

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VE5201	Design for Testability	PCC	3	0	0	3	3
2.	VE5251	CMOS Analog IC Design	PCC	3	0	0	3	3
3.	VE5202	Hardware-Software Co-design of Embedded system	PCC	3	0	0	3	3
4.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
5.	VE5211	Analog System Design Lab	PCC	0	0	4	4	2
			TOTAL	**11**	**0**	**4**	**15**	**11**

*Audit course is optional

SEMESTER – III

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VE5102	VLSI Architectures for System Design	PCC	3	0	0	3	3
2.	VE5104	Real Time Embedded System Design	PCC	3	0	0	3	3
3.	RM5151	Research Methodology and IPR	RMC	2	0	0	2	2
PRACTICALS								
4.	VE5112	Embedded Systems Lab	PCC	0	0	4	4	2
			TOTAL	**8**	**0**	**4**	**12**	**10**

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SEMESTER – IV

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VE5203	Embedded Automation	PCC	3	0	0	3	3
2.		Program Elective I	PEC	3	0	0	3	3
3.		Program Elective II	PEC	3	0	0	3	3
PRACTICALS								
4.	VE5212	Embedded Automation Lab	PCC	0	0	4	4	2
5.	VE5213	Mini Project with Seminar	EEC	0	0	4	4	2
			TOTAL	**9**	**0**	**8**	**17**	**13**

SEMESTER – V

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Program Elective III	PEC	3	0	0	3	3
2.		Program Elective IV	PEC	3	0	0	3	3
3.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
4.	VE5311	Dissertation - I	EEC	0	0	12	12	6
			TOTAL	**9**	**0**	**12**	**21**	**15**

SEMESTER – VI

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICAL								
1.	VE5411	Dissertation - II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 73

PROFESSIONAL CORE COURSES (PCC)

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VE5101	Digital Integrated Circuit Design	PCC	3	0	0	3	3
2.	VE5102	VLSI architectures for system design	PCC	3	0	0	3	3
3.	VE5103	Advanced Embedded System Design	PCC	3	0	0	3	3
4.	VE5104	Real Time Embedded System Design	PCC	3	0	0	3	3
5.	VE5201	Design for Testability	PCC	3	0	0	3	3
6.	VE5251	CMOS Analog IC Design	PCC	3	0	0	3	3
7.	VE5202	Hardware-Software Co-design of Embedded system	PCC	3	0	0	3	3
8.	VE5203	Embedded Automation	PCC	3	0	0	3	3
9.	VE5111	Digital System Design Lab	PCC	0	0	4	4	2
10.	VE5112	Embedded Systems Lab	PCC	0	0	4	4	2
11.	VE5211	Analog System Design Lab	PCC	0	0	4	4	2
12.	VE5212	Embedded Automation Lab	PCC	0	0	4	4	2

FOUNDATION COURSES (FC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	MA5159	Advanced Applied Mathematics	FC	3	1	0	4	4

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EMPLOYABILITY ENHANCEMENT COURSES (EEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VE5311	Dissertation - I	EEC	0	0	12	12	6
2.	VE5411	Dissertation - II	EEC	0	0	24	24	12
3.	VE5213	Mini Project with Seminar	EEC	0	0	4	4	2

RESEARCH METHODOLOGY AND IPR COURSES (RMC)

S. NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	RM5151	Research Methodology and IPR	RMC	2	0	0	2	2

OPEN ELECTIVE COURSES (OEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	OE5091	Business Data Analytics	OEC	3	0	0	3	3
2.	OE5092	Industrial Safety	OEC	3	0	0	3	3
3.	OE5093	Operations Research	OEC	3	0	0	3	3
4.	OE5094	Cost Management of Engineering Projects	OEC	3	0	0	3	3
5.	OE5095	Composite Materials	OEC	3	0	0	3	3
6.	OE5096	Waste to Energy	OEC	3	0	0	3	3

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AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			Lecture	Tutorial	Practical	
1.	AX5091	English for Research Paper Writing	2	0	0	0
2.	AX5092	Disaster Management	2	0	0	0
3.	AX5093	Sanskrit for Technical Knowledge	2	0	0	0
4.	AX5094	Value Education	2	0	0	0
5.	AX5095	Constitution of India	2	0	0	0
6.	AX5096	Pedagogy Studies	2	0	0	0
7.	AX5097	Stress Management by Yoga	2	0	0	0
8.	AX5098	Personality Development Through Life Enlightenment Skills	2	0	0	0
9.	AX5099	Unnat Bharat Abhiyan	2	0	0	0
Total Credits						0

PROGRAM ELECTIVE COURSES (PEC)

S.NO.	COURSE CODE	COURSE TITLE	CATEGORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VE5001	Solid State Device Modeling	PEC	3	0	0	3	3
2.	VE5071	VLSI Signal Processing Techniques	PEC	3	0	0	3	3
3.	VE5002	VLSI For Wireless Communication	PEC	3	0	0	3	3
4.	VL5251	Low Power VLSI Design	PEC	3	0	0	3	3
5.	VL5151	ASIC Design	PEC	3	0	0	3	3
6.	VE5003	SoC Design for Embedded System	PEC	3	0	0	3	3
7.	VE5004	Network on Chip Design	PEC	3	0	0	3	3
8.	VE5005	Advanced CMOS Analog IC Design	PEC	3	0	0	3	3
9.	NE5079	Reconfigurable Architectures and Applications	PEC	3	0	0	3	3
10.	VE5006	Computer Aided Design for VLSI Systems	PEC	3	0	0	3	3
11.	VE5007	Digital Signal Processors and Architectures	PEC	3	0	0	3	3
12.	VE5008	Multi-Core Architectures and Programming	PEC	3	0	0	3	3
13.	NE5074	Image Analysis and Computer Vision	PEC	3	0	0	3	3
14.	VE5009	Quantum Computing	PEC	3	0	0	3	3
15.	NE5251	Adaptive Signal Processing Techniques	PEC	3	0	0	3	3
16.	NE5078	Pattern Recognition and Machine Learning	PEC	3	0	0	3	3
17.	VE5010	Distributed Embedded Computing	PEC	3	0	0	3	3
18.	VE5011	Embedded Networking	PEC	3	0	0	3	3

19.	VE5012	Real Time Operating Systems	PEC	3	0	0	3	3
20.	VE5013	Embedded C Programming	PEC	3	0	0	3	3
21.	VE5014	Embedded Automotive Systems	PEC	3	0	0	3	3
22.	VE5015	MEMS and Microsystems	PEC	3	0	0	3	3
23.	VE5016	RF IC Design	PEC	3	0	0	3	3
24.	NE5071	Computational Intelligence	PEC	3	0	0	3	3
25.	VE5017	Robotics	PEC	3	0	0	3	3

MA5159 **ADVANCED APPLIED MATHEMATICS** **L T P C**
3 1 0 4

OBJECTIVES:

- To encourage students to develop a working knowledge of the central ideas of linear algebra.
- To enable students to understand the concepts of probability and random variables.
- To make students understand the notion of a Markov chain, and how simple ideas of conditional probability and matrices can be used to give a thorough and effective account of discrete-time Markov chains.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To introduce the Fourier Transform as an extension of Fourier techniques on periodic functions and to solve partial differential equations.

UNIT I LINEAR ALGEBRA 12

Vector spaces – norms – Inner Products – Eigenvalues using QR transformations – QR factorization - generalized eigenvectors – Canonical forms – singular value decomposition and applications - pseudo inverse – least square approximations --Toeplitz matrices and some applications.

UNIT II ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT III RANDOM PROCESSES 12

Classification – Auto correlation - Cross correlation - Stationary random process – Markov process –- Markov chain - Poisson process – Gaussian process.

UNIT IV LINEAR PROGRAMMING 12

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V FOURIER TRANSFORM FOR PARTIAL DIFFERENTIAL EQUATIONS 12

Fourier transforms: Definitions, properties-Transform of elementary functions, Dirac Delta functions – Convolution theorem – Parseval‘s identity – Solutions to partial differential equations: Heat equations, Wave equations, Laplace and Poisson‘s equations.

TOTAL: 45+15=60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

- Apply the concepts of linear algebra to solve practical problems.
- Use the ideas of probability and random variables in solving engineering problems.
- Classify various random processes and solve problems involving stochastic processes.
- Formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
- Apply the Fourier transform methods of solving standard partial differential equations.

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REFERENCES:

1. Andrews, L.C. and Philips.R.L., "Mathematical Techniques for engineering and scientists", Printice Hall of India, New Delhi, 2006.
2. Bronson, R., "Matrix Operation", Schaum's outline series, Tata McGrawHill, New York, 2011.
3. O'Neil P.V., "Advanced Engineering Mathematics", Cengage Learning, 8th Edition, India, 2017.
4. Oliver C. Ibe, "Fundamentals of Applied Probability and Random Processes", Academic Press, Boston, 2014.
5. Sankara Rao, K., "Introduction to partial differential equations", Prentice Hall of India, pvt, Ltd, 3rd Edition, New Delhi, 2010.
6. Taha H.A., "Operations Research: An introduction", Ninth Edition, Pearson Education, Asia, 10th Edition, New Delhi, 2017.

VE5101 **DIGITAL INTEGRATED CIRCUIT DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the fundamentals of VLSI design
- To understand the transistor level design of combinational and sequential logic circuits
- To study various memory architectures
- To learn the various arithmetic circuits for data path subsystems
- To familiarize the implementation strategies of FPGA architectures

UNIT - I MOS TRANSISTOR PRINCIPLES 9

MOS Technology and VLSI, CMOS fabrication process and Electrical properties of CMOS circuits – Secondary effects – Device modeling – Process variations – Static and Dynamic behavior of CMOS inverter – Power and Energy – Scaling Principles – Stick Diagram.

UNIT - II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS logic design - Complementary CMOS – Ratioed logic – Pass transistor Logic. Dynamic CMOS logic – principles – speed and power dissipation – signal integrity issues – cascading dynamic gates.

UNIT – III SEQUENTIAL LOGIC CIRCUITS AND MEMORY ARRAY STRUCTURES 9

Static and Dynamic Latches and Registers, Timing Issues, Pipelines, Clocking strategies, Memory Architectures, and Memory control circuits.

UNIT – IV DATAPATH SUBSYSTEMS 9

Introduction – Addition/Subtraction – One/Zero detectors – Comparators – Counters – Coding – Shifters – Multiplication – Division – Parallel-Prefix Computations.

UNIT – V IMPLEMENTATION STRATEGIES 9

DIGITAL: Full custom and semicustom design – cell based design – array based implementation - Programmable ASIC logic cells - ACTEL ACT - Xilinx LCA - Altera FLEX and MAX.

TOTAL: 45 PERIODS

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COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of VLSI design

CO2: Design CMOS combinational and sequential circuits

CO3: Design and analyze various memory architectures

CO4: Analyze characteristics of the datapath/arithmetic circuits

CO5: Analyze Logic block and routing architectures of various FPGAs.

REFERENCES:

1. Jan Rabaey, Anantha Chandrakasan, B.Nikolic, “Digital Integrated circuits: A design perspective”. Second Edition, Prentice Hall of India, 2016.
2. N.Weste, D.M.Harris, “CMOS VLSI Design: Circuits and System Perspective”, Fourth Edition, Pearson, 2015.
3. N.Weste, K.Eshraghian, “Principles of CMOS VLSI Design”, A system Perspective, second edition,Addision Wesley 2010.
4. A.Pucknell, Kamran Eshraghian, “Basic VLSI Design”, Third edition, Prentice Hall of India, 2007.
5. M.J. Smith, “Application specific integrated circuits”, Addisson Wesley, 2009.
6. R.Jacob Baker, Harry W.LI., David E.Boyee, “CMOS Circuit Design, Layout and Simulation”, Prentice Hall of India, 2005.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓			
CO3	✓		✓	✓	✓	
CO4	✓		✓	✓	✓	
CO5	✓		✓	✓	✓	

VE5102 **VLSI ARCHITECTURES FOR SYSTEM DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To introduce the features of programmable logic devices
- To learn the features of various FPGAs and FPAA
- To understand the concepts of synchronous and asynchronous FSMs
- To provide the system design experience with FSMs using PLDs
- To introduce pulse mode approach to asynchronous FSM

UNIT - I PROGRAMMABLE LOGIC DEVICES **9**

Logic implementation options - Technology trends - Design with Field Programmable devices - ROM, PLA, PAL - CPLD - XC9500 family - Erasable Programmable Logic Devices - MAX5000, MAX7000 families.

UNIT - II FPGA AND FPAA 9

Programming Technology, Logic blocks, routing architectures of SRAM-Programmable FPGA Architectures - XC2000, XC3000, XC4000 - Antifuse Programmed FPGAs - Routing Architecture of the Actel FPGAs - ProASIC plus - Design Applications - Current FPGA Technologies - FPAA architecture and its reconfiguration.

UNIT – III SYNCHRONOUS FSM DESIGN 9

Choice of Components to be Considered - Architecture Centered around Nonregistered PLDs - State Machine Designs - Centered around a Shift Register, Centered around a Parallel Loadable Up/Down Counter - One hot design method - Use of Algorithmic State Machine, Application of one hot design to serial 2's complementer, parallel to serial adder/subtractor controller- System-level design: controller, data path, and functional partition.

UNIT – IV ASYNCHRONOUS STATE MACHINE DESIGN 9

Features and need for Asynchronous FSMs - Lumped path delay models for asynchronous FSMs **-** Excitation table, state diagrams, K-maps, and state tables - Design of the basic cells by using the LPD model - design examples - Hazards in Asynchronous FSMs - One-hot design of asynchronous state machines - Design of fundamental mode FSMs by using PLDs.

UNIT – V PULSE MODE APPROACH TO ASYNCHRONOUS FSM DESIGN 9

Pulse Mode Models and System Requirements - Choice of Memory Elements - Other Characteristics of Pulse Mode FSMs - Design Examples - Analysis of Pulse Mode FSMs - One-Hot Programmable Asynchronous Sequencers.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Implement the digital designs with programmable logic devices

CO2: Analyze the architectural features of FPGA and FPAA

CO3: Make the system level designs using synchronous and asynchronous FSMs

CO4: Design the fundamental mode FSMs using PLDs

CO5: Apply pulse mode approach to FSM Design

REFERENCES:

1. Stephen M.Trimberger, Edr.,"Field Programmable Gate Array Technology", Springer Science-Business media, LLC, 2012.
2. Richard F.Tinder, "Engineering Digital Design, Revised Second Edition", Academic Press, 2000.
3. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA-based implementation of Signal Processing Systems", A John Wiley and Sons, Ltd., Publication, 2008.
4. John V. Oldfield, Richard C.Dorf, "Field Programmable Gate Arrays - Reconfigurable logic for rapid prototyping and implementation of digital systems", John Wiley & Sons, Reprint, 2008.
5. P.K.Chan& S. Mourad, "Digital Design Using Field Programmable Gate Array", Prentice Hall, 1994.
6. Thomas L. Floyd, "Electronic Devices", Pearson Education Ltd., 8th Edition, 2008.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓			
CO3	✓		✓	✓	✓	
CO4	✓		✓	✓	✓	
CO5	✓		✓	✓	✓	

VE5103 **ADVANCED EMBEDDED SYSTEM DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the PIC microcontroller and ARM processor architecture, features, pin details and ASM programming
- To develop the programming skills on PIC microcontroller and ARM Processor
- To understand the concepts of real time operating systems
- To learn the interfacing mechanism of peripheral devices with controllers
- To learn the design and development of real-time embedded system

UNIT - I INTRODUCTION **9**

Complex Systems and Microprocessors - Embedded System Design Process - Formalism for System Design - CPU - Programming Input and Output - Supervisor Mode, Exceptions and Traps - Coprocessors - Memory System Mechanism - CPU Bus - CPU performance - CPU Power Consumption.

UNIT - II 8-BIT CONTROLLER **9**

PIC 16F877 MCU - Features - Architecture - Memory - I/O Ports - Timers - ADC - Interrupts - CCP Modules - Instruction set - Assembly language Programming.

UNIT – III 32-BIT CONTROLLER **9**

Fundamentals – Instruction set - Thumb Instruction set - Writing and Optimizing - assembly codes - Efficient C programming - Optimized Primitives - Digital Signal Processing - Exception and Interrupt Handling - Firmware.

UNIT – IV INTERFACING PERIPHERAL DEVICES **9**

Embedded C Programming - LED - LCD - Seven Segment Display - Motor (DC, Stepper, Servo) - Relay - Keypad - Keyboard - Sensors - Serial Communication Protocols (I2C, SPI, USART, CAN), Parallel Communication Protocols (PCI, ISA), Global Positioning System

UNIT – V REAL-TIME OPERATING SYSTEM **9**

The challenges of multitasking and real-time - Achieving multitasking with sequential programming - Operating System Internals - Multitasking Operating Systems - Scheduler Algorithms - Priority Inversion - Tasks, threads and Processes - Exception - Memory model - Memory management address translation - Commercial operating systems - Data and Resource protection - Semaphore - Linux - Disk partitioning.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the PIC microcontroller and ARM Processor architectures
CO2: Write the ASM programming for PIC microcontroller and ARM Processor
CO3: Design the scheduling strategies and resource allocation in RTOS
CO4: Design and develop the hardware and software portion in Real-time embedded Systems
CO5: Port an operating system in Embedded Systems

REFERENCES:

1. Wayne Wolf, "Computers as Components - Principles of Embedded Computing System Design", Morgan Kaufmann Publishers, Second Edition, 2008.
2. Tim Wilmshurst, "Designing Embedded Systems with PIC microcontrollers-Principles and Applications", Newnes Publications, 2007.
3. Muhammad Ali Mazidi, RolinMcKinlay, Danny Causey, "PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications, 2007.
4. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", Morgan Kaufmann Publishers, 2004.
5. Steve Heath, "Embedded Systems Design", Newnes Publications, Second Edition, 2003.
6. Jiacun Wang, "Real-Time Embedded Systems", John Wiley & Sons, Inc, 2017.
7. Phillip A. Laplante, "Real-Time System Design and Analysis", A John Wiley & Sons, Inc, Third Edition, 2004.
8. Tammy Noergaard, "Embedded Systems Architecture - A Comprehensive Guide for Engineers and Programmers", Newnes Publication, 2005.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓	✓		
CO3	✓		✓	✓	✓	
CO4	✓		✓	✓	✓	
CO5	✓		✓			

VE5104 **REAL TIME EMBEDDED SYSTEM DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the basics of embedded system and ARM architecture
- To understand the RTOS concepts like scheduling and memory management related to the embedded system
- To learn about the programming aspects of RTOS
- To learn the different protocols of embedded wireless application
- To understand concepts involved in the design of hardware and software components for an embedded system

Attested

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UNIT I INTRODUCTION **9**

Real Time System – Embedded Systems – Architecture of Embedded System – Simple Programming for Embedded System – Process of Embedded System Development – Pervasive Computing – Information Access Devices – Smart Cards – Microcontrollers – ARM Processor -Real time Microcontrollers.

UNIT II EMBEDDED/REAL TIME OPERATING SYSTEM **9**

Operating System Concepts: Processes, Threads, Interrupts, Events - Real Time Scheduling Algorithms - Memory Management – Overview of Operating Systems for Embedded, Real Time Handheld Devices – Target Image Creation – Programming in Linux, RTLinux, VxWorks, Microcontroller operating system overview.

UNIT III CONNECTIVITY **9**

Wireless Connectivity - Bluetooth – Other short Range Protocols – Wireless Application Environment – Service Discovery – Middleware.

UNIT IV REAL TIME UML **9**

Requirements Analysis – Object Identification Strategies – Object Behaviour – Real Time Design Patterns.

UNIT V SOFTWARE DEVELOPMENT AND APPLICATION **9**

Concurrency – Exceptions – Tools – Debugging Techniques – Optimization –Interfacing Digital Camera with USB port.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

Make a choice of suitable embedded processor for a given application

- Design the hardware and software for the embedded system
- Design and develop the real time kernel/operating system functions, task control block structure and analyze different task states
- Implement different types of inter task communication and synchronization techniques
- To be able to know about the aspects embedded connectivity in real time systems

REFERENCES:

1. R.J.A.Buhr, D.L.Bailey, “An Introduction to Real-Time Systems”, Prentice-Hall International,1999.
2. David E-Simon, “An Embedded Software Primer”, Pearson Education, 2007.
3. C.M.Krishna, Kang G.Shin, “Real Time Systems”, Mc-Graw Hill, 2010.
4. B.P.Douglass, “Real Time UML - Advances in the UML for Real-Time Systems, 3rd Edition, Addison-Wesley, 2004.
5. K.V.K. Prasad, “Embedded/Real Time Systems: Concepts, Design and Programming”, Dream\ Tech Press, Black Book, 2005.
6. R.Barnett, L.O.Cull, S.Cox, “Embedded C Programming and the Microchip PIC”, Thomason Learning, 2004.
7. Wayne Wolf, “Computers as Components - Principles of Embedded Computer System Design”, Mergen Kaufmann Publisher, 2006.
8. Sriram V Iyer, Pankaj Gupta, “Embedded Real Time Systems Programming”, Tata Mc-Graw Hill, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓	✓		✓
CO3	✓		✓	✓	✓	
CO4	✓		✓	✓	✓	
CO5	✓		✓		✓	

RM5151 RESEARCH METHODOLOGY AND IPR LT P C
2 0 0 2

OBJECTIVES:

To impart knowledge and skills required for research and IPR:

- Problem formulation, analysis and solutions.
- Technical paper writing / presentation without violating professional ethics
- Patent drafting and filing patents.

UNIT I RESEARCH PROBLEM FORMULATION 6

Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

UNIT II LITERATURE REVIEW 6

Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III TECHNICALWRITING /PRESENTATION 6

Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) 6

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) 6

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc.
Traditional knowledge Case Studies, IPR and IITs.

TOTAL: 30 PERIODS

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OUTCOMES:

CO1: Ability to formulate research problem
CO2: Ability to carry out research analysis
CO3: Ability to follow research ethics
CO4: Ability to understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity
CO5: Ability to understand about IPR and filing patents in R & D.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓										
CO2	✓											
CO3	✓							✓				
CO4	✓				✓							
CO5	✓					✓						✓

REFERENCES:

1. Asimov, "Introduction to Design", Prentice Hall, 1962.
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners" 2010

VE5111 **DIGITAL SYSTEM DESIGN LAB** **L T P C**
0 0 4 2

OBJECTIVES:

- To learn Hardware Descriptive Language(Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital domain
- To familiarize programming on FPGAs
- To understand the critical design issues of digital logic design
- To provide hands on design experience with professional design (EDA) platforms

LIST OF EXPERIMENTS:

Part I: Module Design using FPGA Implementation (Verilog/VHDL):

1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

Part-II Module Design using ASIC Implementation (Complete Back-End Design):

1. Adders and Subtractors
2. Multiplier (8-bit)

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3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Write HDL code for basic as well as advanced digital integrated circuit
CO2: Import the logic modules into FPGA Boards
CO3: Synthesize Place and Route the digital ICs
CO4: Design various digital IC blocks
CO5: Design, Simulate and Extract the layouts of Digital ICs

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓	✓	✓	✓		✓
CO2	✓	✓	✓	✓	✓	
CO3	✓	✓	✓	✓		✓
CO4	✓	✓	✓	✓		
CO5	✓	✓	✓	✓	✓	

VE5112 EMBEDDED SYSTEMS LABORATORY L T P C
0 0 4 2

OBJECTIVES:

- To learn the basic functions of embedded C programming
- To develop the microcontroller programming skills
- To learn about the development tools
- To learn the interfacing techniques of microcontroller
- To design and develop applications related to embedded systems

8-bit/32-bit Microcontroller based Experiments with:

1. Interfacing basic digital input output devices
2. Interfacing a character LCD
3. Interfacing A/D and D/A converter
4. Interfacing Capture/Compare/PWM module
5. DC motor control
6. Multiplexing seven segment LED displays
7. Interfacing Stepper motor and temperature sensor
8. Traffic light controller using IDE

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Write programming to perform microcontroller operation & its interfacing
CO2: Analyze the basic functions of an embedded system
CO3: Analyze the interfacing circuits for embedded systems
CO4: Design a system to meet desired needs of the environment
CO5: To be able to design and develop real time embedded systems

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓	✓	✓	✓		✓
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓		
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓	✓	

VE5201 **DESIGN FOR TESTABILITY** **L T P C**
3 0 0 3

OBJECTIVES:

- To describe the various fault models and to understand fault detection
- To understand the difficulties of combinational and sequential circuits under test
- To understand the principles of automatic test pattern generation and testable circuit design
- To understand the built in self-test and boundary scan standard
- To understand the testability techniques for system-on-a-chip design

UNIT - I INTRODUCTION TO TESTING **9**

Importance of testing - Testing during the VLSI life cycle - Challenges and levels of abstraction in VLSI testing - VLSI Technology Trends Affecting Testing -Types of testing. Fault Models - Defects, errors, Faults -Stuck-At Faults - Fault Equivalence, Fault Collapsing, Fault Dominance- Transistor Faults, Open and Short Faults, Delay Faults, Pattern Sensitivity and Coupling Faults - Analog Fault Models- Automatic test Equipment.

UNIT - II LOGIC AND FAULT SIMULATION **9**

SCOAP Testability Analysis **-** Algorithms for True Value simulation **-** Compiled-Code Simulation, Event-Driven Simulation - Algorithms for Fault Simulation - Serial Fault Simulation, Parallel Fault Simulation, Deductive Fault Simulation, Concurrent Fault Simulation, Roth's TEST-DETECT Algorithm, Differential Fault Simulation.

UNIT – III ATPG FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS **9**

Combinational Circuit: Algorithms and Representations, Redundancy Identification (RID), Combinational ATPG Algorithms - D-Calculus and D-Algorithm, PODEM and FAN.
Sequential Circuit: ATPG for Single-Clock Synchronous Circuits, Time-Frame Expansion Method, Simulation-Based Sequential Circuit ATPG -CONTEST Algorithm, Genetic Algorithm.

UNIT – IV DFT METHODS AND BUILT-IN SELF-TEST **9**

DFT Methods - Ad Hoc Approach, Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow.
BIST - Design Rules - Test Pattern Generation - Output Response Analysis - Logic BIST Architectures - Fault Coverage Enhancement - BIST Timing Control - Logic BIST System Design - A Design Practice - Memory BIST.

UNIT – V BOUNDARY SCAN STANDARD AND CORE-BASED TESTING 9

Core-Based Design and Test Considerations - Digital Boundary Scan - IEEE Std. 1149.1 - Test Architecture and Operations, Test Access Port and Bus Protocols, Data Registers and Boundary-Scan Cells, TAP Controller - Embedded Core Test Standard (IEEE Std. 1500) - Architecture, Wrapper Components and Functions - Comparisons between 1500 and 1149.1 Standards.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design and simulate the fault models
CO2: Apply fault simulation algorithms for circuit under test
CO3: Design test pattern generation circuits for combinational and sequential circuits
CO4: Design built-in-self test for circuit under test
CO5: Analyze the testability techniques for Embedded core design

REFERENCES:

1. M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory, and Mixed Signal VLSI Circuits - Kluwer Academic Publishers, Reprint 2013.
2. L.T. Wang, C.W. Wu and X. Wen, VLSI Test Principles and Architectures, Elsevier, 2006.
3. Samiha Mourad, Yervant Zorian, “Principles of Testing Electronic Systems”, A Wiley Interscience Publications, 2002.
4. Alexander Miczo, “Digital Logic Testing and Simulation”, Second Edition, A John Wiley & Sons Inc. Publication, 2003.
5. Abramovici, M, Breuer, M.A and Friendman, A.D., ”Digital systems and Testing and Testable Design”, Computer Science Press 1990.
6. Alfred Crouch, “Design for test for digital IC & Embedded Core Systems”, Prentice Hall, 2002

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓	✓	✓
CO2	✓		✓			
CO3	✓		✓	✓	✓	
CO4	✓		✓	✓	✓	
CO5	✓		✓			

VE5251 CMOS ANALOG IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To learn the equivalent circuits and models of MOS circuits
- To analyze various biasing circuits
- To design and analyze various differential amplifier architectures
- To design and analyze the frequency response of various differential amplifiers
- To discuss the stability and frequency compensation of feedback amplifiers

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UNIT - I SINGLE STAGE AMPLIFIERS 9

Review of MOS physics and equivalent circuits and models. Large and Small signal analysis CS, CG and source follower, miller effect, frequency response of CS, CG and source follower.

UNIT - II CURRENT MIRRORS 9

Current Sources, Basic Current Mirrors, Cascode stages for Current mirrors, Wilson Current Mirror,Widler Current Mirror Large and small signal analysis of current mirrors.

UNIT – III MULTISTAGE DIFFERENTIAL AMPLIFIERS 9

Differential amplifier, Large and small signal analysis of the balanced differential amplifier, device mismatches in differential amplifier, small and large signal analysis of the differential pair with current mirror load, $PSRR^+$, $PSRR^-$ and CMRR of differential amplifiers, small signal analysis of telescopic amplifier, two-stage amplifier and folded cascoded amplifier.

UNIT – IV FREQUENCY RESPONSE OF MULTISTAGE DIFFERENTIAL AMPLIFIERS 9

Frequency response of differential amplifier-transfer function method, Miller effect, Dominant-Pole approximation, Upper Cutoff frequency-zero-value time constant method,UGF-short circuit time constant method, frequency response of telescopic cascoded, folded cascaded and two-stage amplifiers.

UNIT – V STABILITY AND FREQUENCY COMPENSATION OF FEEDBACK AMPLIFIERS 9

Properties and types of negative feedback circuits, feedback configurations, effect of loading in feedback networks, feedback circuit analysis using return ratio modelling input and output port in feedback network, the relation between gain and bandwidth in feedback amplifiers, phase margin, frequency compensation, compensation of two stage MOS amplifiers.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze and design CMOS analog IC building blocks

CO2: Design the various current mirror biasing circuits

CO3: Analyze and Design the various single and multistage differential amplifier architectures

CO4: Analyze the frequency response of single and multi-stage differential amplifiers

CO5: Analyze and design various feedback amplifiers with compensation

REFERENCES:

1. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits” Fifth Edition John Wiley, 2016.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Twelfth Reprint, Tata McGraw Hill, 2012.
3. Phillip E. Allen, Douglas R.Holberg, “CMOS Analog Circuit Design”, Third edition, Oxford University Press, 2011.
4. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation, Third Edition”, Wiley IEEE Press 2010.
5. Kenneth William Martin, David Johns, “Analog Integrated Circuit Design”, , Wiley India, 2008.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓	✓	
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓		

VE5202 HARDWARE - SOFTWARE CO-DESIGN OF EMBEDDED SYSTEM L T P C
3 0 0 3

OBJECTIVES:

- To introduce the key concepts of hardware/software communication
- To learn the data flow implementation in software and hardware
- To learn the concept of integration of custom hardware components with software
- To learn the design space of custom architectures
- To understand the design and implementation experience with case studies

UNIT - I NATURE OF HARDWARE AND SOFTWARE 9

Hardware, Software, Definition of Hardware/Software Co-Design – Driving factors Platform design space – Application mapping – Dualism of Hardware design and software design – Concurrency and parallelism, Data flow modeling and Transformation – Data Flow Graph – Tokens, actors and queues, Firing rates, firing rules and Schedules – Synchronous data flow graph – control flow modeling – Adding time and resources – Transformations.

UNIT - II DATA FLOW IMPLEMENTATION IN SOFTWARE AND HARDWARE 9

Software Implementation of Data Flow – Converting queues and actors into software, Dynamic Scheduler – Hardware Implementation of Data Flow – single rate SDF graphs into hardware, Pipelining – Analysis of control flow and data flow – construction of control and data flow graph – Translating C into hardware – Designing data path and controller.

UNIT – III DESIGN SPACE OF CUSTOM ARCHITECTURES 9

Finite state machines with datapath – FSMD design example, Limitations – Microprogrammed Architecture – Microprogrammed control, microinstruction encoding, Microprogrammed data path, microprogrammed machine – General purpose Embedded Core – RISC pipeline, Program organization – SoC interfaces for custom hardware – Design Principles in SoC Architecture

UNIT – IV HARDWARE/ SOFTWARE INTERFACES 9

Principles of Hardware/software communication – synchronization schemes, communication constrained versus Computation constrained, Tight and Loose coupling - On-chip buses – Memory mapped interfaces – coprocessor interfaces – custom instruction interfaces – Coprocessor hardware interface – Data and control design, programmer's model.

UNIT – V Applications 9

Zynq processor-centric platforms-Scalable Processor Architecture, Trivium for 8-bit platforms – AES coprocessor, CORDIC coprocessor – algorithm and implementation

Attested

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the key concepts in hardware/software co-design

CO2: Analyze the data flow implementation in software and hardware

CO3: Design the fundamental building blocks using hardware/software co-design and related implementation

CO4: Design and analyze with modern hardware/software tools for building prototypes of embedded systems

CO5: Analyze the various processors

REFERENCES:

1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 2010.
2. Jorgen Staunstrup, Wayne Wolf, "Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub, 2013.
3. Giovanni De Micheli, Rolf Ernst Morgon, "Reading in Hardware/Software Co-Design" Kaufmann Publishers, 2002.
4. Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2nd Edition, Springer, 2014.
5. Louise H. Crockett, "Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC" Strathclyde Academic Media,2014

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓		✓	
CO3	✓		✓	✓		
CO4	✓		✓	✓		
CO5	✓		✓		✓	✓

VE5203 **EMBEDDED AUTOMATION** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn about the process involved in the design and development of real-time embedded system
- To develop the Embedded C programming skills on 8-bit microcontroller
- To study about the interfacing mechanism of peripheral devices with 8-bit microcontrollers
- To learn about the tools, firmware related to microcontroller programming
- To build a home automation system

UNIT - I INTRODUCTION TO EMBEDDED C PROGRAMMING **9**

C Overview an Program Structure - C types, Operators and Expressions - C control flow - C functions and Program Structures - C pointers and arrays - FIFO and LIFO - C Structures - development tools

UNIT - II AVR MICROCONTROLLER **9**

Atmega16 Architecture - Nonvolatile and Data memories - Port System - Peripheral features : Time base, Timing Subsystem, Pulse width modulation, USART, SPI, Two wire serial Interface, ADC, Interrupts - Physical and operating parameters

UNIT – III HARDWARE AND SOFTWARE INTERFACING WITH 8-BIT SERIES CONTROLLERS **9**

Lights and Switches - Stack operation - Implementing Combinational logic - Expanding I/O - Interfacing Analog to Digital Convertors - Interfacing Digital to Analog Convertors - LED Displays : Seven segment displays, Dot matrix displays - LCD Displays - Driving Relays - Stepper Motor interface - Serial EEPROM - Real Time Clock - Accessing Constants Table - Arbitrary Waveform Generation - Communication links - System Development tools

UNIT – IV VISION SYSTEM **9**

Fundamentals of Image Processing - Filtering - Morphological Operations - Feature detection and Matching - Blurring and Sharpening - Segmentation - Thresholding - Contours - Advanced Contour Properties - Gradient - Canny Edge Detector - Object Detection - Background Subtraction

UNIT – V HOME AUTOMATION **9**

Home automation - Requirements - Water level notifier - Electric guard dog - Tweeting bird feeder - Package delivery detector - Web enabled light switch - Curtain automation - Android door lock - Voice controlled home automation - Smart Lighting - Smart Mailbox - Electricity usage monitor -Proximity garage door opener - Vision based authentic entry system

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the 8-bit series microcontroller architecture, features and pin details
CO2: Write Embedded C programs for embedded system application
CO3: Design and develop real time systems using AVR microcontrollers
CO4: Design and develop the systems based on vision mechanism
CO5: Design and develop a real time home automation system

REFERENCES:

1. Dhananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", McGraw-Hill, 2001.
2. Joe Pardue, "C programming for Microcontrollers ", Smiley Micros, 2005.
3. Steven F. Barrett, Daniel J. Pack, "Atmel AVR Microcontroller Primer : Programming and Interfacing", Morgan & Claypool Publishers, 2008.
4. Mike Riley, "Programming your Home - Automate with Arduino, Android and your computer", The Pragmatic Programmers, LLC, 2012.
5. Richard Szeliski, "Computer Vision: Algorithms and Applications", Springer, 2011.
6. Kevin P. Murphy, "Machine Learning - A Probabilistic Perspective", The MIT Press Cambridge, Massachusetts, London, 2012.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓	✓	✓			
CO3	✓		✓	✓		
CO4	✓		✓	✓	✓	Attested
CO5	✓		✓	✓	✓	

VE5211 **ANALOG SYSTEM DESIGN LAB** **L T P C**
0 0 4 2

OBJECTIVES:

- To learn the principles of CMOS amplifiers
- To design single stage amplifiers and current mirror circuits
- To understand multistage amplifiers and their design constrains
- To provide hands on design experience with professional design (EDA) platforms
- To design analog hardware blocks using FPAA

LIST OF EXPERIMENTS:

Part I: Module Design and Simulation using Analog Design Environment

1. Design of Common Source Amplifier
2. Design of Cascade and Cascode amplifiers
3. Design of current Mirrors
4. Design of differential pair amplifier with active load
5. Design of telescopic amplifier circuit
6. Design of two-stage amplifier circuit

Part II: Layout extraction and simulation using Analog Design Environment

7. Layout generation, parasitic extraction and layout simulation for experiments 1 to 3.

Part-III Analog block hardware design using FPAA

1. Design of variable gain amplifier
2. Filtering Audio signal from noises using notch filter
3. Analyzing frequency response of Band pass filter
4. Monitoring Heart rate signal using PPG sensor

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

- Design basic and advanced analog circuits
- Design and simulate various amplifiers
- Import the standard cells in analog domain
- Synthesize Place and Route the analog ICs
- Design and analyze various analog blocks using FPAA

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓	✓	✓	✓		✓
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓	✓	

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VE5212 **EMBEDDED AUTOMATION LAB** **L T P C**
0 0 4 2

OBJECTIVES:

- To learn about the design and development of different automation systems
- To enhance the Embedded C programming skills
- To study about the interfacing mechanism of peripheral devices with microcontrollers
- To improve the programming skills related to Computer vision
- To build a home automation system

LIST OF EXPERIMENTS:

1. Water level controller
2. Unauthorized entry identifier
3. Tweeting bird feeder
4. Package delivery detector
5. Web enabled light switch
6. Curtain automation
7. Android door lock
8. Voice controlled home automation
9. Smart Lighting
10. Smart Mailbox
11. Proximity garage door opener

TOTAL: 60 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design and develop real time systems using microcontrollers
CO2: Design and develop the systems based on vision mechanism
CO3: To be able to build large, complex systems
CO4: Design and develop a real time home automation system
CO5: Students should be able to know the different embedded tools

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓	✓	✓	✓		✓
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓	✓	
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓		

VE5001 **SOLID STATE DEVICE MODELING** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the basic concepts of solid semiconductors
- To understand the principle behind all types of device modeling
- To learn and understand different noise models of devices
- To analyze the device performance in terms of mathematical expressions
- To comprehend the widely used device models in industry such as BSIM and EKV

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UNIT - I MOSFET DEVICE PHYSICS 9

Introduction to solids, Bonding forces and energy bands in solid semiconductors, MOS capacitor - Interface Charge, threshold voltage, MOS Capacitance, MOS Charge control model, MOS Operation and characteristics. MOSFET fabrication process.

UNIT - II MOSFET MODELING 9

Basic MOSFET Modeling-Meyer model, velocity saturation model, capacitance model, Basic small signal model. Advanced MOSFET Modeling-modeling approach, High field effects, short channel effects,Gate leakage and effective oxide thickness, Unified MOSFET C–V Model- Unified Meyer C–V model, Ward–Dutton model, Non-quasi-static modeling.

UNIT – III RF AND NOISE MODELING 9

RF modeling of MOS transistors- Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling. Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, modeling for accurate distortion analysis-nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuit.

UNIT – IV BSIM4 MOSFET MODELING 9

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, Mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, Noise model, Junction diode models , Layout-dependent parasitics model.

UNIT – V OTHER MOSFET MODELS 9

The EKV model- model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, temperature effects, MOS model 9, MOSAI model, Influence of process variation, Modeling of device mismatch for Analog/RF Applications.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the concepts and procedural flow that are used to construct the complicated device models
CO2: Design and analyze different MOSFET models
CO3: Analyze the noise models of MOSFET
CO4: Analyze the design challenges involved in device models
CO5: Analyze the EKV and BSIM4 MOSFET models

REFERENCES:

1. Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd, 2003
2. Yannis Tsividis and Colin McAndrew, "Operation and Modelling of the MOS transistor", Cambridge University Press, 2011.
3. A. B. Bhattacharyya, "Compact MOSFET Models for VLSI Design", John Wiley & Sons Inc., 2009.
4. Streetman and Banerjee, Semiconductor Physics and Devices, 6th Edition, Pearson Prentice Hall, 2006.
5. Rudan, Massimo, "Physics Of Semiconductor Devices", Springer International Publishing, 2017.

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	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓		✓	✓
CO2	✓		✓	✓		
CO3	✓		✓		✓	
CO4	✓		✓		✓	
CO5	✓		✓		✓	

VE5071 VLSI SIGNAL PROCESSING TECHNIQUES L T P C
3 0 0 3

OBJECTIVES:

- To understand the overview of DSP systems and the concepts of parallel and pipeline techniques
- To acquire knowledge on various retiming algorithms and architectures
- To acquire knowledge on fast convolution algorithms
- To understand the architecture of parallel and pipelined recursive filters
- To develop knowledge on the clocking styles of the digital circuits

UNIT - I INTRODUCTION TO DSP SYSTEMS, PIPELINING AND PARALLEL PROCESSING FOR FIR FILTERS 9

Overview of DSP systems – FPGA Technology- DSP Technology Requirements- Data flow and Dependence graphs - Critical path, Loop bound, Iteration bound, Longest path matrix Algorithm, Pipelining and Parallel Processing of FIR filters.

UNIT - II RETIMING, ALGORITHMIC STRENGTH REDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application, Algorithmic strength reduction in filters and transforms – Parallel FIR filter - Fast FIR algorithms - Parallel Architectures for Rank-order filters - Odd-Even merge-sort architecture, parallel rank-order filters.

UNIT – III FAST CONVOLUTION, PIPELINED AND PARALLEL RECURSIVE AND ADAPTIVE FILTERS 9

Fast convolution – Cook-Toom algorithms, Winograd algorithms, Pipelined and parallel recursive filters – Pipeline Interleaving in Digital Filters- Pipelining in I & II order Digital Filter – Parallel Processing for IIR Filter- Pipelined Adaptive Digital Filters.

UNIT – IV BIT-LEVEL ARITHMETIC ARCHITECTURES 9

Parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers - Design of Lyon‟s bit-serial multipliers using Horner‟s rule, Bit-serial FIR filter design - CSD Arithmetic, CSD multiplication using Horner‟s rule for precision improvement - Distributed Arithmetic - Offset binary coding.

UNIT – V NUMERICAL STRENGTH REDUCTION, SYNCHRONOUS, WAVE AND ASYNCHRONOUS PIPELINING 9

Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression sharing - Synchronous pipelining and Clocking styles - Clock skew in edge-triggered single phase clocking and Two-phase clocking - Wave Pipelining - NPCPL - Asynchronous Pipelining.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the critical path of the DSP architectures
CO2: Design efficient retiming architecture for FIR filter using data flow graphs
CO3: Analyze various bit-level arithmetic architectures used in signal processing applications
CO4: Design fast convolution algorithms to minimize computational complexity
CO5: Analyze and implement proper clocking techniques on VLSI circuits

REFERENCES:

1. Keshab K. Parhi, “VLSI Digital Signal Processing Systems, Design and implementation “, Wiley, Interscience, 2007.
2. U. Meyer Baese, “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, Second Edition, 2013.
3. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA-based Implementation of Signal Processing Systems", Digital Signal and Image Processing Series, A John Wiley and Sons, Ltd., Publication, 2017.
4. Roger Woods, John McAllister, Gaye Lightbody and Ying Yi, "FPGA-based Implementation of Signal and Data Processing Systems**",** Wiley, 2017.
5. Shoab Ahmed Khan, "Digital Design of Signal Processing Systems - A Practical Approach", A John Wiley and Sons, Ltd., Publication, 2011.
6. Lars Wanhammar, "DSP Integrated Circuits", Academic Press, 1999.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓		✓	✓
CO2	✓		✓	✓		
CO3	✓		✓		✓	
CO4	✓		✓	✓		
CO5	✓		✓		✓	

VE5002 **VLSI FOR WIRELESS COMMUNICATION** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the concepts of basic wireless communication systems
- To study the parameters in receiver and low noise amplifier design
- To study the various types of mixers and PLLs design for wireless communication
- To understand the concepts of transmitters and power amplifiers used in wireless communication
- To discuss the architectures of wireless transceivers at the transistor level

UNIT - I COMMUNICATION CONCEPTS **9**

Introduction – Overview of Wireless systems – Standards – Access Methods – Modulation schemes – Classical channel – Wireless channel description – Path loss – Multipath fading.

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UNIT - II TRANSMITTER AND RECEIVER ARCHITECTURES 9

Transmitter back end design – Quadrature LO generator, Receiver front end – Filter design – Non-idealities – Design parameters – Noise figure & Input intercept point. LNA Introduction – Wideband LNA design – Narrow band LNA design: Impedance matching & Core amplifier.

UNIT – III MIXERS 9

Active Mixer: Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Noise - A Complete Active Mixer.

Passive Mixer: Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNIT – IV ANALOG TO DIGITAL CONVERTERS 9

Demodulators – A/D converters used in receivers – Low-pass and band-pass sigma delta modulators and its implementation-I/Q mismatch in converters

UNIT – V FREQUENCY SYNTHESIZERS 9

PLL – Phase detector – Dividers – Voltage Controlled Oscillators – LC oscillators – Ring Oscillators – Phase noise – Loop filters & design approaches – A complete synthesizer design example (DECT).

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Apply the VLSI concepts in wireless communication techniques
CO2: Design and analyze the LNA and Mixers
CO3: Design and analyze PLL for real time applications
CO4: Analyze the characteristics of receivers and frequency synthesizers
CO5: Design and analyze A/D converters

REFERENCES:

1. Bosco H Leung “VLSI for Wireless Communication”, Second Edition, Springer, 2014.
2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,2012.
3. BehzadRazavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 2016.
4. Emad N Farag and Mohamed I Elmasry, “Mixed Signal VLSI wireless design – Circuits & Systems”, Kluwer Academic Publishers, 2000.
5. J. Crols and M. Steyaert, “CMOS Wireless Transceiver Design,” Boston, Kluwer Academic Pub., 2013.
6. Thomas H.Lee, “The Design of CMOS Radio – Frequency Integrated Circuits”, Cambridge University Press ,2004.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓		✓	✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓		

VL5251 **LOW POWER VLSI DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- Identify sources of power in an IC.
- Identify the power reduction techniques based on technology independent and technology dependent methods
- Identify suitable techniques to reduce the power dissipation.
- Estimate Power dissipation of various MOS logic circuits.
- Develop algorithms for low power dissipation.

UNIT I POWER DISSIPATION IN CMOS **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9**

Logic level power optimization – Circuit level low power design – Gate level low power design – Architecture level low power design – VLSI subsystem design of adders, multipliers, PLL, low power design.

UNIT III DESIGN OF LOW POWER CMOS CIRCUITS **9**

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNIT IV POWER ESTIMATION **9**

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis –Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER **9**

Synthesis for low power – Behavioral level transform –Algorithms for low power – software design for low power.

TOTAL: 45 PERIODS

OUTCOMES:

CO1: Ability to find the power dissipation of MOS circuits
CO2: Design and analyse various MOS logic circuits
CO3: Apply low power techniques for low power dissipation
CO4: Able to estimate the power dissipation of ICs
CO5: Ability to develop algorithm to reduce power dissipation by software.

REFERENCES:

1. Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2. J.B.Kulo and J.H Lou, “Low voltage CMOS VLSI Circuits”, Wiley 1999.
3. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer,1995.
4. Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.
5. Abdelatif Belaouar, Mohamed.I.Elmasry, “Low power digital VLSI design”, Kluwer, 1995.
6. James B.Kulo, Shih-Chia Lin, “Low voltage SOI CMOS VLSI devices and Circuits”, John Wiley and sons, inc. 2001.
7. J.Rabaey, “Low Power Design Essentials (Integrated Circuits and Systems)”, Springer, 2009

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	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	2	3	1	2	2
CO2	3	3	2	1	2	1
CO3	1	2	1	2	1	1
CO4	1	2	2	1	2	2
CO5	2	3	2	2	2	1

VL5151 **ASIC DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- The course focuses on the semi-custom IC Design and introduces the principles of design logic cells, I/O cells and interconnect architecture, with equal importance given to FPGA and ASIC styles.
- The entire FPGA and ASIC design flow is dealt with from the circuit and layout design point of view.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN **9**

Types of ASICs - Design flow - CMOS transistors - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS **9**

Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC ARCHITECUTRE **9**

Architecture and configuration of Artix / Cyclone and Kintex Ultra Scale / Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT IV LOGIC SYNTHESIS, PLACEMENT AND ROUTING **9**

Logic synthesis - Floor Planning Goals and Objectives, Measurement of Delay in floor planning, Floor planning tools ,I/O and Power planning, Clock planning, Placement Algorithms. Routing: Global routing, Detailed routing ,Special routing.

UNIT V SYSTEM-ON-CHIP DESIGN **9**

SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High performance filters using delta-sigma modulators.
Case Studies: Digital camera, SDRAM, High speed data standards.

TOTAL: 45 PERIODS

OUTCOMES:

CO1: Ability to apply logical effort technique for predicting delay, delay minimization and FPGA architectures
CO2: Ability to design logic cells and I/O cells
CO3: Ability to analyze the various resources of recent FPGAs
CO4: Ability to use algorithms for floorplanning and placement of cells and to apply routing algorithms for optimization of length and speed.
CO5: Ability to analyze high performance algorithms available for ASICs

REFERENCES:

1. M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
2. Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science.
3. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008
4. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. Douglas J. Smith, HDL Chip Design, Madison, AL, USA: Doone Publications, 1996.
6. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994 28
7. S.Pasricha and N.Dutt,” On-Chip Communication Architectures System on Chip Interconnect, Elsveir”, 2008

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		2	1		
CO2	3		2	1		
CO3	3		2	1		
CO4	3		3	2	1	1
CO5	3		3	2	1	1

VE5003 SoC DESIGN FOR EMBEDDED SYSTEM L T P C
3 0 0 3

OBJECTIVES:

- To learn the basics of system-on-chip
- To learn architecture and design concepts underlying system on chips
- To impart knowledge about the hardware-software design of a modest complexity chip all the way from specifications, modeling, synthesis and physical design
- To learn the memory circuits
- To understand various interconnect architectures of SoC design

UNIT - I SYSTEM ARCHITECTURE: OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system level interconnection – SoC design requirements and specifications – design integration – design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processor design, Configurability.

UNIT - II PROCESSOR SELECTION FOR SOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interrupts and exceptions. Basic elements in instruction handling – Minimizing pipeline delays – reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNIT – III MEMORY DESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategies for line replacement at miss time – split I- and D- caches – multilevel caches – SoC memory systems – board based memory systems – simple processor/memory interaction.

UNIT – IV INTERCONNECT ARCHITECTURES AND SOC CUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect – Processor customization approaches – Reconfigurable technologies – mapping designs onto reconfigurable devices - FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNIT – V FPGA BASED EMBEDDED PROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors and Hard Processors – Tool flow for Hardware/Software Co-design –Interfacing Processor with memory and peripherals – Types of On-chip interfaces – Wishbone interface, Avalon Switch Matrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the components of a System-on-Chip and an embedded system
CO2: Analyze the major design flows for digital hardware and embedded software
CO3: Design and analyze the major architectures and trade-offs of chips and embedded systems
CO4: Design and analyze various interconnect architectures
CO5: Design memory circuits for embedded system applications

REFERENCES:

1. Michael J. Flynn and Wayne Luk**,** “Computer System Design: System-on-Chip”, John Wiley and sons, 2011.
2. Rahul Dubey, “Introduction to Embedded System Design Using Field Programmable Gate Arrays”, Springer Verlag London Ltd., 2009.
3. Sudeep Pasricha and Nikil Dutt, On-Chip Communication Architectures - System on Chip Interconnect”, Elsevier, 2008.
4. Michael Keating and Pierre Bricaud, "Reuse Methodology Manual for System -On-A-Chip Designs", Third Edition, Kluwer Academic Publishers, 2002.
5. "Embedded Design Handbook - FPGA CPLD and ASIC", Intel, 2018.

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	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓			✓
CO2	✓		✓			
CO3	✓		✓	✓		
CO4	✓		✓	✓	✓	
CO5	✓		✓	✓	✓	

VE5004 **NETWORK ON CHIP DESIGN** **L T P C**
3 0 0 3

OBJECTIVES:

- To impart knowledge in the concept of a peer to peer interconnection network, shared bus based design, and network on chip (NoC) based architectures
- To address the issues of scalability of on-chip connectivity and inter processor communication
- To introduce the types of networks and performance analysis
- To understand the quality of service provided by NoC
- To analyze various performance metrics of NoC

UNIT - I INTRODUCTION TO INTERCONNECTION NETWORKS 9

Uses of Interconnection Networks, Network Basics, A Simple Interconnection Network, Network Specifications and Constraints, Topology, Routing, Flow Control, Router Design, Performance Analysis.

UNIT - II TYPES OF NETWORKS 9

Butterfly Networks, Torus Networks Mesh Networks,Non-blocking networks, Non-interfacing networks, Crossbar networks Clos Networks, Beneˇs Networks, Sorting Networks

UNIT – III ROUTING & FLOW CONTROL 9

Routing Basics, Deterministic Routing, Dimension-Order Routing, Adaptive Routing, Adaptive Routing Basics, Minimal Adaptive Routing, Fully Adaptive Routing, Flow control basics, Butterflow control, Buffer Management and Back pressure, A flit reservation flow control, Deadlock and livelock avoidances, Deadlock and livelock avoidances in adaptive routing

UNIT – IV QUALITY OF SERVICE & ROUTER 9

Guranteed services, Best-Effort services, Router Datapath Components, Input Buffer organization, Switches, Output Organization, Arbitration, waveform allocator, Processor-Network Interface, Shared-Memory Interface.

UNIT – V PERFORMANCE ANALYSIS 9

Throughput, Latency, Fault Tolerance, Common Measurement Pitfalls Queuing Theory, Probabilistic Analysis, Application-Driven Workloads, Synthetic Workloads, Virtual Channels, Network Size, Injection Processes, Prioritization, Stability, Fault tolerance.

TOTAL: 45 PERIODS

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OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design various networks by considering design constrains

CO2: Design and Analyze the various types of networks

CO3: Design the routing and flow control in networks

CO4: Analyze the various performance metrics

CO5: Design the quality of service and routing mechanisms

REFERENCES:

1. William James Dally and Brian Patrick Towles, “Principles and Practices of Interconnection Networks”,The Morgan Kaufmann Series in Computer Architecture and Design,2004.
2. Sudeep Pasricha and Nikil Dutt, “On-Chip Communication Architectures - System on Chip Interconnect”, Elsevier, 2010.
3. Jih-Sheng Shen and Pao-Ann Hsiung, “Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication”, IGI global, 2010.
4. Umit Y. Ogras and Radu Marculescu, " Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures", Springer, 2013.
5. Santanu Kundu Santanu Chattopadhyay, " Network-on-Chip - The Next Generation of System-on-Chip Integration", CRC Press, Taylor & Fracis Group, 2015.
6. Stavroula N.Ventoura, "NOC Switch Design and Simulation using Matlab’s Simulink", Master Thesis, National And Kapodistrian University of Athens, 2013.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓		

VE5005 ADVANCED CMOS ANALOG IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To understand various sources of noises in Analog Blocks
- To understand various OTA architectures
- To understand the switched-capacitor circuits and data conversion circuits
- To learn and design bandgap reference circuits
- To learn the performance metrics involved in analog IC design

UNIT - I NOISE IN INTEGRATED CIRCUITS 9

Statistical Characteristics of Noise, Sources of noise, noise models of IC components, Circuit noise calculations, equivalent input noise generators, effect of feedback on noise performance, noise in CS, CE, CG and cascode amplifiers, noise in differential pair, noise bandwidth.

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UNIT - II OTA DESIGN CONSIDERATION 9

Step response, Slewing, OTA variations, CMFB implementation, Input resistance, Output resistance, Output Voltage swing, CMRR, PSRR of two-stage telescopic amplifiers.

UNIT – III BANDGAP REFERENCE CIRCUIT AND SWITCHED CAPACITOR CIRCUITS 9

Supply Insensitive biasing, Temperature insensitive biasing, Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

UNIT – IV PERFORMANCE METRICS OF DATA CONVERTERS & NYQUIST RATE D/A CONVERTERS 9

Ideal Sampling, Reconstruction, Quantization, Static performance metrics, Dynamic performance metrics, Current Steering DACs, capacitive DACs, Binary weighted versus thermometer DACs.

UNIT – V ANALOG TO DIGITAL CONVERTERS 9

Single stage amplifier as comparator, resistor-based latched comparators. offset cancellation, Flash ADC, Successive approximation ADC, Pipelined ADC, Time Interleaved ADC.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design various analog block by considering noises and their effects

CO2: Design various OTA architectures and CMFB block

CO3: Design and analyze bandgap reference circuits

CO4: Analyze switched-capacitor circuits and the issue of non-linearity and mismatch in the circuits

CO5: Analyze data conversion circuits such as DAC and ADC and their design techniques.

REFERENCES:

1. Gray, Hurst, Lewis, Meyar, “Analysis and Design of Analog Integrated Circuits”, Fifth Edition John Wiley, 2016.
2. BehzadRazavi, “Design of Analog CMOS Integrated Circuits”, Twelfth Reprint, Tata McGraw Hill, 2012.
3. Rudy Van de Plassche, “CMOS Integrated ADC and DACs” 2nd Edition, Springer,2007
4. Phillip E.Allen, DouglasR.Holberg, “CMOS Analog Circuit Design”, Third edition, Oxford University Press, 2011.
5. Jacob Baker “CMOS: Circuit Design, Layout, and Simulation”, Third Edition, Wiley IEEE Press 2010.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓	✓	
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓		

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NE5079 RECONFIGURABLE ARCHITECTURES AND APPLICATIONS L T P C
3 0 0 3

OBJECTIVES:

- The student shall develop an overview and deeper insight into the research and development that is underway to meet future needs of flexible processors
- To learn the concepts of implementation, synthesis and placement of modules in reconfigurable architectures
- To understand the communication techniques and system on programmable chip for reconfigurable architectures
- To learn the process of reconfiguration management
- To familiarize the applications of reconfigurable architectures

UNIT - I INTRODUCTION 9

General purpose computing – domain specific processors – application specific processors – reconfigurable computing – fields of application – evolution of reconfigurable systems – simple programmable logic devices – complex programmable logic devices – field programmable gate arrays – coarse grained reconfigurable devices.

UNIT - II IMPLEMENTATION, SYNTHESIS AND PLACEMENT 9

Integration – FPGA design flow – Logic synthesis – LUT based technology mapping – modeling – temporal partitioning algorithms – offline and online temporal placement – managing device's free and occupied spaces.

UNIT – III COMMUNICATION AND SoPC 9

Direct communication – communication over third party – bus based communication – circuit switching – network on chip – dynamic network on chip – system on a programmable chip – adaptive multi-processing on chip.

UNIT – IV RECONFIGURATION MANAGEMENT 9

Reconfiguration – configuration architectures – managing the reconfiguration process – reducing configuration transfer time – configuration security.

UNIT – V APPLICATIONS 9

FPGA based parallel pattern matching - Low power FPGA based architecture for microphone arrays in wireless sensor networks - Exploiting partial reconfiguration on a dynamic coarse grained reconfigurable architecture – Parallel pipelined OFDM baseband modulator with dynamic frequency scaling for 5G systems.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the different architecture principles relevant to reconfigurable computing systems

CO2: Compare the tradeoffs that are necessary to meet the area, power and timing criteria of reconfigurable systems

CO3: Analyze the algorithms related to placement and partitioning

CO4: Analyze the communication techniques and system on programmable chip for reconfigurable architectures

CO5: Analyze the principles of network and system on a programmable chip

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REFERENCES:

1. Christophe Bobda, “Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications”, Springer 2007.
2. Scott Hauck and Andre Dehon, “Reconfigurable Computing: The Theory and Practice of FPGA based Computation”, Elsevier 2008.
3. M. Gokhale and P. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005.
4. Nikoloas Voros et al. “Applied Reconfigurable Computing: Architectures, Tools and Applications” Springer, 2018.
5. Koen Bertels, João M.P. Cardoso, Stamatis Vassiliadis, “Reconfigurable Computing: Architectures and Applications”, Springer 2006.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓	✓		
CO3	✓		✓		✓	
CO4	✓		✓		✓	
CO5	✓		✓		✓	

VE5006 COMPUTER AIDED DESIGN FOR VLSI SYSTEMS L T P C
3 0 0 3

OBJECTIVES:

- To learn the Algorithmic Graph Theory and computational complexity optimization
- To analyze the concepts of layout design rules and floor planning
- To analyze the algorithms on floor planning and routing
- To learn high level synthesis and scheduling algorithm
- To simulate and synthesis different hardware models

UNIT - I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of VLSI Design automation tools – Graph theory and computational complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT - II LAYOUT COMPACTION, PLACEMENT AND PARTITIONING 9

Design rules – Symbolic layout - Problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – wire length estimation – types of placement problem - Placement algorithms – partitioning.

UNIT – III FLOOR PLANNING AND ROUTING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems -Area routing - channel routing - Global routing: introduction and algorithms.

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UNIT – IV SIMULATION AND LOGIC SYNTHESIS 9

Gate level modeling and simulation – Switch level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT – V HIGH LEVEL SYNTHESIS 9

Hardware models - Internal representation of input algorithms – Allocation - Assignment - scheduling – scheduling algorithms - assignment problems - high level transformations.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Implement, simulate and synthesis the computer aided design of VLSI systems
CO2: Analyze the Algorithmic Graph Theory and computational complexity optimization
CO3: Analyze the concepts of layout design rules and floor planning
CO4: Design and optimize circuits using various graphical algorithms
CO5: Simulate and synthesis different hardware models

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, Reprint - 2008.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2013.
3. Christoph Meinel and Thorsten Theobald, "Algorithms and Data structures in VLSI Design - OBDD Foundations and Applications", Springer Verlag, Berlin Heidelberg, New York, 1998.
4. Prithviraj Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design", Prentice Hall Inc., 1994.
5. Shin-ichi Minato, "Binary Decision Diagrams And Applications for VLSI CAD", Kluwer Academic Publishers, First edition, 1996.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓		✓	
CO3	✓		✓		✓	
CO4	✓		✓	✓		
CO5	✓		✓		✓	

VE5007 DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES L T P C 3 0 0 3

OBJECTIVES:

- To understand the architecture and programming of fixed and floating point DSP processors
- To understand the techniques involved in real time DSP system design
- To learn and design the basic forms of FIR and IIR filters
- To understand the fast implementation schemes of DFT
- To understand the structures and algorithms of adaptive filters

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UNIT - I INTRODUCTION TO DIGITAL SIGNAL PROCESSING SYSTEMS 9

Fundamentals of DSP - Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT - II FIXED AND FLOATING POINT DIGITAL SIGNAL PROCESSORS 9

TMS320C55x – Architecture overview, Addressing modes, Instruction set, Programming considerations, system issues. TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Realtime implementations.

UNIT – III FAST FOURIER TRANSFORMS 9

Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation usingTMS320C64x, Floating point implementation using TMS320C67x.

UNIT – IV FIR AND IIR FILTER IMPLEMENTATIONS 9

FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation usingTMS320C64x, Floating point implementation using TMS320C67x.

UNIT – V ADAPTIVE FILTER STRUCTURES AND ALGORITHMS 9

Wiener filter, LS filter , Filter structures, Adaptive algorithms, Properties and Applications – Fixed and floating point implementation using TMS320C64x and TMS320C67x.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Develop the program for fixed and floating point DSP processors based on the design issues
CO2: Design and develop real time implementations on DSP algorithms
CO3: Design IIR and FIR filters with desired frequency responses
CO4: Apply the fast transforms for the analysis of DSP systems
CO5: Analyze the structures and algorithms of adaptive filters

REFERENCES:

1. Sen M.Kuo, Woon-Seng S.Gan, “Digital Signal Processors – Architectures, Implementations and Applications”, Pearson Education, 2005, Second Impression, 2009.
2. Lapsley et al “DSP Processor Fundamentals, Architectures & Features”, S.Chand & Co, 2000, Reprint.
3. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, Wiley, 2009.
4. John G Proakis and Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson, Fourth Edition, 2007.
5. TMS Manual on TMS320C64XX and TMS320C67XX.
6. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.
7. S.K. Mitra, “Digital Signal Processing, A Computer Based approach", Tata McGraw-Hill,2006.
8. P. Vaidyanathan, “Multirate Systems & Filter Banks", Prentice Hall, 1993.
9. I.C.Ifeachor and B.W. Jervis, “Digital Signal Processing-A Practical Approach”, Pearson, 2002.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓		✓	✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓		✓	

VE5008 **MULTICORE ARCHITECTURES AND PROGRAMMING** **L T P C 3 0 0 3**

OBJECTIVES:

- To learn the basics of multicore processing
- To understand the principles of parallel programming
- To understand the principles of different multiprocessors with their performance issues
- To understand the fundamentals of various programming concepts used in multicore architectures
- To learn the concepts of multicore architectures for embedded systems

UNIT - I INTRODUCTION TO MULTIPROCESSORS AND SCALABILITY ISSUES **9**

Scalable design principles – Principles of processor design – Instruction Level Parallelism, Thread level parallelism. Parallel computer models –- Symmetric and distributed shared memory architectures – Performance Issues – Multi-core Architectures - Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture.

UNIT - II PARALLEL PROGRAMMING **9**

Fundamental concepts – Designing for threads – scheduling - Threading and parallel programming constructs – Synchronization – Critical sections – Deadlock. Threading APIs.

UNIT – III OPENMP PROGRAMMING **9**

OpenMP – Threading a loop – Thread overheads – Performance issues – Library functions. Solutions to parallel programming problems – Data races, deadlocks and livelocks – Non-blocking algorithms – Memory and cache related issues.

UNIT – IV MPI PROGRAMMING **9**

MPI Model – collective communication – data decomposition – communicators and topologies – point-to-point communication – MPI Library.

UNIT – V MULTICORE ARCHITECTURES FOR EMBEDDED SYSYETMS **9**

Architectural Considerations, Interconnection Networks, Software Optimizations. Case Studies: HiBRIDSoC for Multimedia Signal Processing, VIPER MultiprocesssorSoC, General Purpose Multiprocessor DSP, Multicore DSP Platforms.

TOTAL: 45 PERIODS

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OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of multicore processing

CO2: Analyze the principles of parallel programming

CO3: Analyze the principles of different multiprocessors with their performance issues

CO4: Analyze the fundamentals of various programming concepts used in multicore architectures

CO5: Design the concepts of multicore architectures for embedded systems

REFERENCES:

1. ShameemAkhter and Jason Roberts, “Multi-core Programming”, Intel Press, 2006.
2. Michael J Quinn, Parallel programming in C with MPI and OpenMP, Tata Mcgraw Hill, 2004.
3. GeorgiosKornaros, “Multicore Embedded systems”, CRC Press, Taylor & Francis Group, 2010.
4. John L. Hennessey and David A. Patterson, “ Computer architecture – A quantitative approach”, Morgan Kaufmann/Elsevier Publishers, 4th. edition, 2017.
5. David E. Culler, Jaswinder Pal Singh, “Parallel computing architecture : A hardware/ software approach” , Morgan Kaufmann/Elsevier Publishers, 2000.
6. Bryon Moyer, “Real world Multicore Embedded systems”, Elsevier, 2013.
7. GerassimosBarlas, “Multicore and GPU Programming: An Integrated Approach”, Elsevier, 2015.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓		✓	✓
CO2	✓		✓		✓	
CO3	✓		✓		✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓		

NE5074 **IMAGE ANALYSIS AND COMPUTER VISION** **L T P C**
3 0 0 3

OBJECTIVES:

- To introduce to basic concepts and methodologies for digital image processing
- To learn the various image transform techniques
- To understand the general processes of image enhancement, segmentation, representation and description
- To learn the principles of image compression
- To understand the various computer vision based applications

UNIT - I IMAGE ENHANCEMENT 9

Digital image fundamentals - Image sampling - Quantization - Spatial domain filtering - intensity transformations - Contrast stretching - Histogram equalization - Smoothing filters, Sharpening filters - Noise distributions - Mean filters - Order statistics filters

UNIT - II IMAGE TRANSFORMS 9

1D DFT- 2D Transforms - DFT- DCT- Walsh - Hadamard - Slant - Haar - KLT- SVD- Wavelet transform

UNIT – III IMAGE RESTORATION AND SEGMENTATION 9

Image restoration - degradation model - Unconstrained and Constrained restoration - Inverse filtering - Wiener filtering - Image segmentation - Thresholding - Edge detection, Edge linking - Region based methods

UNIT – IV IMAGE COMPRESSION 9

Need for data compression - Huffman - Arithmetic coding - LZW technique - Vector Quantization - JPEG – MPEG

UNIT – V VIDEO PROCESSING 9

Back ground Subtraction - Video analytics - Video object Segmentation - Object Detection - Face Recognition - Motion Estimation

TOTAL: 45 PERIODS

OUTCOMES:

CO1: To be able to implement image enhancement algorithms
CO2: To be able to apply image transform for different imaging modalities
CO3: To be able to perform different segmentation and restoration processes
CO4: To be able to implement different compression techniques
CO5: To be able to develop algorithms for computer vision problems

REFERENCES:

1. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson Education, Inc., Third Edition, 2007
2. Anil K. Jain, "Fundamentals of Digital Image Processing”, Prentice Hall of India, 2004.
3. Milan Sonka, Vaclav Hlavac and Roger Boyle, “Image Processing, Analysis and Machine Vision”, Brookes/ Cole, Vikas Publishing House, 2nd edition,1999.
4. Sid Ahmed, M.A., “ Image Processing Theory, Algorithms and Architectures”, Mc Graw Hill, 1995.
   Richard Szeliski, "Computer Vision - Algorithms and Applications", Springer Verlag London Limited, 2011.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓		✓	
CO3	✓		✓		✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓		

VE5009 **QUANTUM COMPUTING** **L T P C**
3 0 0 3

OBJECTIVES:

- To familiar with the concepts of quantum logic
- To learn the quantum computing basics and algorithms
- To learn the reversible logic circuits
- To understand various architectural elements and its programming techniques
- To design the sequential circuits using reversible logic gates

UNIT - I QUANTUM COMPUTATIONS AND ALGORITHMS 9

Introduction – signal states – logic operations – quantum measurement – integer factorization – order finding – phase and eigen value estimation - hidden subgroup problem – grover's and adiabatic algorithms.

UNIT – II QUANTUM ARCHITECTURES AND SIMULATION 9

Reliable and realistic implementation technology – robust error correction and fault tolerant structures – quantum resource distribution – simulation of error propagation – stabilizer method.

UNIT – III ARCHITECTURAL ELEMENTS AND PROGRAMMING 9

Processing elements – memory hierarchy – addressing schemes – architecture design – Quantum array logic architecture – Programming: physical level instruction scheduling – high level compiler design – architecture independent circuit synthesis – mapping – optimization.

UNIT – IV REVERSIBLE LOGIC: FUNDAMENTALS AND SYNTHESIS 9

Reversible logic gates – synthesis – expansions and spectral transforms – garbage elimination-decision trees and diagrams – lattice and fast transformation circuits – group theoretic representations – reconstructability analysis – reversible programmable gate array – evaluation.

UNIT – V REVERSIBLE SEQUENTIAL LOGIC CIRCUITS 9

Reversible flip flops – complex reversible sequential circuits – novel reversible elements – multiple valued circuits.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basics of quantum computing
CO2: Design and analyze quantum architectures and algorithms
CO3: Design and simulate the basic elements using quantum computing
CO4: Design reversible logic circuits
CO5: Design and analyze sequential circuits using reversible logic

REFERENCES:

1. Saleem Mohammed RidhaTaha, "Reversible Logic Synthesis Methodologies with Application to Quantum Computing" Springer, 2016.
2. Tzvetan S. Metodi, Arvin I. Faruque and Frederic T. Chong, "Quantum Computing for Computer Architects" Second Edition, Morgan and Claypool Publishers, 2011.
3. Jennifer Chubb, Ali Eskandarian, Valentina Harizanov, "Logic and Algebraic Structures in Quantum Computing" Series: Lecture Notes in Logic, Cambridge University Press, 2016.
4. Bernard Zygelman, "A First Introduction to Quantum Computing and Information" Springer 2018.
5. Aboul Ella Hassanien, Mohamed Elhoseny and Janusz Kacprzyk, "Quantum Computing: An Environment for Intelligent Large Scale Real Application" Springer 2018.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓		✓	

NE5251 **ADAPTIVE SIGNAL PROCESSING TECHNIQUES** **L T P C 3 0 0 3**

OBJECTIVES:

- To understand the basic principles of discrete random signal processing
- To understand the principles of spectral estimation
- To learn about the weiner and adaptive filters
- To understand the different signal detection and estimation methods
- To acquire skills to design synchronization methods for proper functioning of the system

UNIT - I DISCRETE RANDOM SIGNAL PROCESSING 9

Discrete Random Processes, Random variables, Parseval's theorem, Wiener-Khintchine relation, Power Spectral Density, Spectral factorization, Filtering Random Processes, Special types of Random Processes.

UNIT - II SPECTRAL ESTIMATION 9

Introduction, Nonparametric methods – Periodogram, Modified periodogram, Bartlett, Welch and Blackman-Tukey methods, Parametric methods – ARMA, AR and MA model based spectral estimation, Solution using Levinson-Durbin algorithm.

UNIT – III WEINER AND ADAPTIVE FILTERS 9

Weiner Filter: FIR wiener filter, IIR wiener filter**,** Adaptive Filter: FIR adaptive filters – Steepest descent method- LMS algorithm, RLS adaptive algorithm, Applications.

UNIT – IV DETECTION AND ESTIMATION 9

Bayes detection techniques, MAP, ML,– detection of M-ary signals, NeymanPeason, minimax decision criteria. kalman filter- Discrete kalman filter, The Extended kalman filter, Application.

UNIT – V SYNCHRONIZATION 9

Signal parameter estimation, carrier phase estimation, symbol timing estimator, joint estimation of carrier phase and symbol timing.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the basic principles of discrete random signal processing

CO2: Analyze the principles of spectral estimation

CO3: Analyze the weiner and adaptive filters

CO4: Analyze the different signal detection and estimation methods

CO5: Design the synchronization methods for proper functioning of the system

REFERENCES:

1. Monson H. Hayes, “Statistical Digital Signal Processing and Modeling”, John Wiley and Sons, Inc, Singapore, 2009.
2. John G. Proakis., "Digital Communication", 4 th edition, McGraw Hill Publication, 2001.
3. Simon Haykin, “Adaptive Filter Theory”, Pearson Education, Fourth Edition, 2003.
4. Bernard Sklar and Pabitra Kumar Roy, “Digital Communications: Fundamentals and Applications”, 2/E, Pearson Education India, 2009
5. Paulo S. R. Diniz, “Adaptive Filtering Algorithms and Practical Implementation”, Springer, 2011.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓		✓	
CO3	✓		✓		✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓		

NE5078 PATTERN RECOGNITION AND MACHINE LEARNING L T P C
3 0 0 3

OBJECTIVES:

- To understand the basics of data processing and dimensionality reduction techniques
- To understand different learning models for classification
- To understand the principles and applications of ANN architectures
- To study the different Deep convolutional networks
- To learn deep generative models

UNIT - I BASICS OF PROBABILITY AND RANDOM PROCESS 9

Probability Theory - Conditional and Joint Probability - Stationary and non-stationary process - Expectation - Auto correlation - Cross Correlation - Eigen values - Eigen vectors - Singular values - Singular vectors - Decision Theory - Information Theory

UNIT - II DIMENSIONALITY REDUCTION 9

Introduction - Features, feature vectors - Feature selection and ranking - Discriminant functions - Fisher’s Discriminant analysis - Principal Component Analysis - Kernel PCA - Independent component analysis

LEARNING MODELS 9

UNIT – III

Linear models for Classification and Regression - Classifiers based on Bayes Decision theory – Naïve Bayes - Nearest neighbor rules - Mixture models - Mixture of Gaussian - Hidden Markov Model

UNIT – IV ARTIFICIAL NEURAL NEWORKS 9

Supervised Learning - Unsupervised Learning- Reinforcement Learning – Feed Forward and Feedback architectures - Multilayer Perceptron - Backpropagation Algorithm- Radial Basis Function networks - Support vector Machines

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UNIT – V DEEP LEARNING NETWORKS **9**

Introduction to Deep neural networks – Convolution neural networks – Deep Belief Networks - Recurrent neural networks

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1:Employ different feature extraction and dimensionality reduction techniques
CO2: Design different learning models
CO3: Implement different neural network architectures
CO4: Realize basic Deep neural network architectures
CO5: Test and implement deep generative models for various data processing applications

REFERENCES:

1. Christopher M. Bishop, " Pattern Recognition and Machine Learning", Springer2011
2. R.O. Duda, P.E. Hart and D.G. Stork, "Pattern Classification" John Wiley, 2002
3. EthemAlpaydm, "Introduction to Machine Learning", Second Edition, The MIT Press, Cambridge, 2010.
4. Kevin P. Murphy, "Machine Learning - A Probabilistic Perspective", The MIT Press, Cambridge, 2012.
5. Josh Patterson and Adam Gibson, "Deep Learning - A Practitioner's Approach", O'Reilly Media, Inc, 2017.
6. Richard Szeliski, "Computer Vision - Algorithms and Applications", Springer Verlag London Limited, 2011.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓	✓	✓	
CO3	✓		✓		✓	
CO4	✓		✓			
CO5	✓		✓	✓	✓	

VE5010 DISTRIBUTED EMBEDDED COMPUTING **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the fundamentals of Network communication technologies.
- To understand the fundamentals of Internet
- To study on Java based Networking
- To introduce network routing Agents
- To learn the basis for network on-chip technologies

UNIT - I THE HARDWARE INFRASTRUCTURE **9**

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT - II INTERNET IN EMBEDDED COMPUTING 9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT – III DISTRIBUTED COMPUTING USING JAVA 9

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT – IV EMBEDDED AGENT 9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent-Mobile robots.

UNIT – V EMBEDDED COMPUTING ARCHITECTURE 9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the fundamentals of Network communication technologies
CO2: Analyze the internet and Java based networking
CO3: Design and analyze the network routing agents
CO4: Analyze the various network-on-chip technologies
CO5: Analyze the analog/digital co-design of distributed embedded computing architecture

REFERENCES:

1. Dietel & Dietel, “JAVA how to program”, Prentice Hall 2017.
2. Sape Mullender, “Distributed Systems”, Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, “Distributed Systems – concepts and design”,Addison Wesley 1988.
4. “Architecture and Design of Distributed Embedded Systems”, edited by Bernd Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001
5. M. Teresa Higuera-Toledano and Andy J. Wellings, " Distributed, Embedded and Real-time Java Systems", Springer, 2012.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓	✓	

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VE5011 **EMBEDDED NETWORKING** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the concepts of Serial and parallel communication protocols
- To understand the application development using USB and CAN bus for PIC microcontrollers
- To learn the basics of ethernet
- To learn the application development using embedded internet
- To learn the wireless sensor network communication protocols

UNIT - I COMMUNICATION PROTOCOLS 9

Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - PCI Bus protocol.

UNIT - II USB AND CAN BUS 9

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC Microcontroller USB Interface – CAN Bus – Introduction - Basic Concepts & Definitions-Identifiers & Arbitration-Robustness & Flexibility-Message Formats-Error Handling -PIC microcontroller CAN Interface –A simple application with CAN.

UNIT – III ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT – IV EMBEDDED ETHERNET 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP.

UNIT – V EMBEDDED WIRELESS SENSOR NETWORKS 9

Wireless sensor networks –Introduction to WSN-Challenges for WSNs - Characteristic requirements - Required mechanisms - Single-node architecture -Hardware components-Energy consumption of sensor nodes-Operating systems and execution environments-Some examples of sensor nodes.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the wired and wireless network protocols
CO2: Design an application using embedded networking
CO3: Analyze the basics of Ethernet
CO4: Incorporate networks in embedded systems
CO5: Analyze the basics of wireless sensor networks

REFERENCES:

1. Frank Vahid, Tony Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction” - John & Wiley Publications, 2006
2. Jan Axelson, “Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port” - Penram Publications, 1996.
3. Dogan Ibrahim, “Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series” - Elsevier 2008.

4. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram publications, 2003.
5. Bhaskar Krishnamachari, Networking, Wireless Sensors - Cambridge press 2005.
6. Olaf Pfeiffer, Andrew Ayre and Christian Keydel, “Embedded Networking with CAN and CAN open”, Second edition published by Copperhill Media Corporation, 2003.
7. Holgerkarl, Andreas Willig, “Protocols and architectures for wireless sensor networks”, John Wiley,2005

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		•
CO2	✓		✓	✓	✓	
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓	✓		

VE5012 REAL TIME OPERATING SYSTEMS L T P C
3 0 0 3

OBJECTIVES:

- To learn about significance and usage of Real time operating system
- To learn about different scheduling strategies and optimization principles
- To learn about the resource allocation or sharing process involved in RTOS
- To study about the different firmware and tools related to RTOS development
- To design and develop an innovative real time embedded system

UNIT - I REAL TIME EMBEDDED SYSTEMS 9

Introduction - History of Real time systems and Embedded systems - Real time services and standards - System resources - Analysis - Service utility - Scheduling Classes - Cyclic executive - Scheduler concepts- Real time operating System - Thread safe Reentrant Functions

UNIT - II RESOURCES AND SERVICES 9

Processing - Resources - Memory –Multiresource services : Blocking, Deadlock, livelock, Critical sections to protect shared resources, Priority inversion, Power management and Processor clock modulation - Soft real time services : Missed deadlines, Quality of Service, Alternatives to Rate monotonic policy, Mixed hard and soft real time services

UNIT – III REAL TIME EMBEDDED COMPONENTS 9

Hardware components - Firmware components - RTOS system software - Software application components - Traditional Hard real time operating systems : Asymmetric Multicore Processing and Symmetric Multi-core Processing - Processor core affinity - SMP support models - RTOS Hypervisors - Open source real time operating systems

UNIT – IV INTEGRATING EMBEDDED LINUX 9

Integrating Embedded Linux into Real time systems - Debugging Components - Performance tuning - High availability and Reliability Design - Hierarchical approaches for fail-safe design

UNIT – V CASE STUDIES 9

System life cycle - Continuous Media applications - video and audio processing - Robotic applications - Computer vision applications

Attested

TOTAL: 45 PERIODS

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OUTCOMES:

On successful completion of this course, students will be able to

CO1: Complete understanding of scheduling algorithm and process

CO2: Better understanding on firmware and tools related to the development of RTOS

CO3: To be able to design and develop an embedded system with RTOS functionality

CO4: To be able to design and develop the systems in Linux environments

CO5: To be able to develop large real-time embedded systems

REFERENCES:

1. Sam Siewert, John Pratt, "Real-time embedded components and systems with Linux and RTOS", Mercury Learning and Information LLC, 2016.
2. Jonathan W. Valvano, "Embedded Systems: Real time operating systems for ARM Cortex-M Microcontrollers", Createspace Independent Publishing Platform, Fourth Edition, 2017.
3. Giorgio C. Buttazzo, "Hard Real-Time Computing Systems - Predictable Scheduling Algorithms and Applications", Springer Science+Buisness Media, LLC, Third Edition, 2011.
4. Albert M. K. Cheng, "Real-Time Systems - Scheduling, Analysis and Verification", A John Wiley & Sons INC Publication, 2002.
5. Wang K.C., “Embedded and Real Time Operating System”, Springer, 2017

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓	✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓	✓	

VE5013 **EMBEDDED C PROGRAMMING** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the process involved in the design and development of real-time embedded system
- To develop the programming skills on PIC microcontroller
- To study the interfacing mechanism of peripheral devices with controllers
- To learn the tools, firmware and programming methodologies related to embedded system design
- To improve the knowledge base and programming skill of students in Real time embedded system

UNIT - I INTRODUCTION **9**

C Overview an Program Structure - Constants - Preprocessor Directives - Data Variables and Types - Expression and Operators - Statements - Functions - Arrays - Structures - Memory and Pointers - Built in Functions - Strings - Function like Macros - Conditional Compilation

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UNIT - II 8-BIT MICROCONTROLLER 9

8-bit Microcontroller - Features - Architecture - Memory Organization - I/O Ports - Timers - Watchdog Timers - ADC - Interrupts - RESET - CCP Modules - USART - I2C - SPI - Parallel Slave Port

UNIT – III CONFIGURATION AND PROGRAMMING 9

Minimal Hardware Connection - Device Programming - Hex Files - Power up Considerations - Clock Configuration - Integrated Development Environment -Debugging - Bootloading - Real Time Methods - Using Interrupts - State Machines

UNIT – IV INTERFACING PERIPHERAL DEVICES 9

LED - LCD - Seven Segment Display - Motor (DC, Stepper, Servo) - Relay - Keypad - Keyboard - Sensors -, Global Positioning System - External Serial Buses - RS232 - RS422 - RS485 -USB - CAN - LIN

UNIT – V RTOS PROGRAMMING & CASE STUDIES 9

Multitasking Operating Systems - Preemptive Scheduling - Dispatcher Scheduling - Deterministic Scheduling - Data and Resource protection - Semaphore - Message Passing - await () - Task management - Commercial operating systems - Linux - Disk partitioning - Tank Water Level Controller, Bank visitor counter - Digital Multimeter - Electronic Scooter

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design a system with embedded C programming and debugging skills
CO2: Interface the peripheral device with microcontroller
CO3: Analyze the scheduling strategies, resource allocation and process methods involved in RTOS
CO4: Design and develop the hardware and software portion in Real-time embedded Systems
CO5: Design and develop innovative real time systems

REFERENCES:

1. Mark Siegesmund, "Embedded C Programming - Techniques and Applications of C and PIC MCUs", Newnes is an imprint of Elsevier, First Edition, 2014.
2. Tim Wilmshurst, "Designing Embedded Systems with PIC microcontrollers-Principles and Applications", Newnes Publications, 2007.
3. Muhammad Ali Mazidi, Rolin McKinlay, Danny Causey, "PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18", Prentice Hall publications, 2007.
4. Richard Barnett, Larry O'Cull, Sarah Cox, "Embedded C Programming with the Microchip PIC", Delmar Learning, a division of Thomson Learning, 2004.
5. Phillip A. Laplante, "Real-Time System Design and Analysis", A John Wiley & Sons, Inc, Third Edition, 2004.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓			
CO3	✓		✓	✓		
CO4	✓		✓	✓	✓	
CO5	✓		✓	✓	✓	

Attested

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VE5014	EMBEDDED AUTOMOTIVE SYSTEMS	L T P C 3 0 0 3

OBJECTIVES:

- To learn the Fundamentals of Electronic Components related to automotive applications
- To learn on Automotive Sensors, Actuators and Instrumentations
- To learn the Control Mechanisms in an Automotive System
- To learn about the automotive instrumentation system
- To learn Telematics and Diagnostic methods

UNIT - I SYSTEMS APPROACH TO CONTROL AND INSTRUMENTATION 9

System, Linear system theory, Steady-State sinusoidal frequency response of a system, State variable formulation of models, Control theory, Stability of Control System, Closed-Loop Limit-Cycle Control, Instrumentation, Basic Measurement System, Filtering, Digital Subsystem, Sinusoidal Frequency Response, Discrete Time Control System, Closed loop control, Example Discrete Time Control System.

UNIT - II FUNDAMENTALS OF ELECTRONICS, MICROCOMPUTER INSTRUMENTATION AND CONTROL 9

Semiconductor Devices, Transistors, ICs, Operational Amplifiers, Use of Feedback in Op Amps, Phase-Locked Loop, Digital Circuits, Logic Circuits (Combination and Sequential Circuits), Timers and Counters, Microcomputer fundamentals, Tasks and Operations, CPU Registers, Reading Instructions, Programming Languages, Microcomputer Hardware, Microcomputer Applications in Automotive Systems, Instrumentation Applications of Mirocomputers, Microcomputers in Control Systems.

UNIT – III SENSORS, ACTUATORS AND ELECTRONIC ENGINE CONTROL 9

Motivation for Electronic Engine Control, Exhaust Emissions, Fuel Economy, Test Procedures, Concept of an Electronic Engine Control System, Engine Performance Terms, Exhaust Catalytic Convertors, Electronic Fuel-Control System, Analysis of Intake Manifold Pressure, Idle Speed Control, Electronic Ignition, Automotive Control System Applications of Sensors and Actuators, Throttle Angle Sensor, Temperature Sensor, Coolant Sensor, Sensors for Feed back control, Knock Sensors, Automotive Engine Control Actuators, Variable Valve Timing, Electric Motor Actuators, Ignition System.

UNIT – IV MOTION AND DIGITAL POWERTRAIN CONTROL SYSTEM 9

Digital Engine Control, Features, Control Modes for Fuel Control, Discrete Time Idle Speed Control, EGR Control, Variable Valve Timing Control, Electronic Ignition Control, Integrated Engine Control System, Summary of Control Modes, Cruise Control System, Cruise Control Electronics, Antilocking Braking System, Electronic Suspension System, Electronic Steering Control, Four-Wheel Steering.

UNIT – V AUTOMOTIVE INSTRUMENTATION, TELEMATICS AND ITS DIAGNOSTICS 9

Modern Automotive Instrumentation, Input and Output Signal Generation, Advantages of Computer Based Instrumentation, Display Devices, Flat Panel Display, Fuel Quantity Measurement, Coolant Temperature Measurement, Oil Pressure Measurement, Vehicle Speed Measurement, High-Speed Digital Communication (CAN BUS), Telematics, GPS Navigation, GPS System Structure, Automotive Diagnostics.

TOTAL: 45 PERIODS

Attested

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze with the fundamentals of Electronic Components related to automotive applications

CO2: Design Automotive Sensors, Actuators and Instrumentations

CO3: Analyze the Control Mechanisms in an Automotive System

CO4: Analyze the operations of Telematics and Diagnostic methods

CO5: To be able to understand the complete automotive operation and control mechanisms

REFERENCES:

1. William B. Ribbens, "Understanding Automotive Electronics- An Engineering Prespective", 7th Edition, Butterworth-Heinemann Publications, 2012.
2. Young A.P. & Griffiths, " Automotive Electrical Equipment" , ELBS & New Press,1999.
3. Tom Weather Jr. &Cland c. Ilunter, " Automotive computers and control system", Prentice Hall Inc., New Jersey.
4. Crouse W.H., " Automobile Electrical Equipment" , McGraw Hill Co. Inc., New York ,1995.
5. Bechhold, " Understanding Automotive Electronic", SAE,1998.
6. Robert Bosch," Automotive Hand Book", SAE, 5TH Edition,2000.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓			
CO3	✓		✓	✓		
CO4	✓		✓	✓	✓	
CO5	✓		✓	✓		

VE5015 **MEMS AND MICROSYSTEMS** **L T P C**
3 0 0 3

OBJECTIVES:

- To understand the fundamentals of MEMS and Microsystems
- To understand the micro mechanism of MEMs
- To learn MEMS accelerometers and actuators design techniques
- To understand the concepts of MEMS interfacing
- To familiarize with some MEMS applications

UNIT - I INTRODUCTION TO MEMS **9**

MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT - II MICROMECHANICS **9**

Elasticity, Stress, strain and material properties, Bending of thin films, Spring configurations, torsion deflection, Mechanical vibration, Resonance, Thermomechanics - actuators, force and response time, Fracture and thin film mechanics.

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UNIT – III MICROACTUATORS 9

Electrostatics: basic theory, electrostatic instability. Surface tension, Gap and finger pull up, Electrostatic actuators, comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators, bistable actuators.

UNIT – IV INTERFACING AND PACKAGING 9

Electronic Interfaces, Feedback systems, Noise, Packaging: Dicing-Wafer level Packaging-Wafer bonding-Connections between layers-self assembly-higher level of packaging.

UNIT – V CASE STUDIES 9

Optical MEMS, RF MEMS- System design basics, Case studies: Capacitive accelerometer, Peizo electric pressure sensor, MEMS scanners, Capacitive RF MEMS switch, performance issues.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to
CO1: Analyze the working of MEMS and Microsystems components
CO2: Analyze the principles of micromechanism
CO3: Design and analyze the interfacing of MEMS and microsystems
CO4: Design the MEMS accelerometer and to design Electrostatic actuators
CO5: Analyze the working of RF and Optical MEMS

REFERENCES:

1. Stephen D Senturia, "Microsystems Design", 2nd edition Springer Publishers, 2013.
2. Nadim Maluf and Kirt Williams, "Introduction to Micro electromechanical Systems Engineering", Artech House, 2004.
3. Mohamed Gad-el-Hak, Editor, "The MEMS Handbook", 2nd Edition, CRC press, 2005.
4. Tai - Ran Hsu, "MEMS and Micro Systems: Design, Manufacture and Nanoscale Engineering", 2nd Edition, Tata McGraw Hill, New Delhi, 2008.
5. Ville Kaajakarrai, " Practical MEMS",Small Gear Pub., 2009

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓	✓	✓	
CO5	✓		✓		✓	

VE5016 RF IC DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To understand the fundamentals of RF integrated circuits operating at microwave frequencies
- To learn the circuit design for low noise amplifiers
- To understand the concepts of power amplifier design
- To learn the fundamentals of PLL and frequency synthesizers
- To learn RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology

UNIT - I COMPONENTS FOR RF IC **9**

MOSFET Physics: Long channel and Short channel approximation, Noise: Two port Noise theory,MOS capacitor, Spiral Inductors, Model for on chip inductors,Bond wire inductors, Monolithic transformer realization, Interconnects.

UNIT - II CIRCUIT DESIGN FOR LOW NOISE AMPLIFIERS **9**

Methods of Open circuit and Short circuit time constants, Bandwidth enhancers, Tuned amplifier, Neutralisation, cascaded amplifiers, CMOS amplifiers, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.

UNIT – III POWER AMPLIFIER DESIGN **9**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations , Compensation, Class A, AB, B, C, D, E and F amplifiers, Linearization Techniques, RF power amplifier design example.

UNIT – IV PLL AND FREQUENCY SYNTHESIZERS **9**

Linearized PLL Model, Noise properties, Phase detectors, Loop filters and Charge pumps, PLL Design examples. Integer-N frequency synthesizers, Direct Digital Frequency synthesizers.

UNIT – V SYSTEM ARCHITECUTRE **9**

Receiver architecture: Noise figure, Linearity in cascaded systems,Single and Dual conversion receivers, Image reject receivers, Direct conversion. Transmitter architectures, Detailed Chip design example: WLAN Transceiver architecture.

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the fundamentals of RF integrated circuits operating at microwave frequencies
CO2: Design the circuit for low noise amplifiers
CO3: Design the circuit for power amplifier
CO4: Analyze the fundamentals of PLL and frequency synthesizers
CO5: Analyze RFIC design techniques, including system architecture, key building blocks design methodologies in CMOS technology

REFERENCES:

1. Thomas Lee, “The Design of Radio Frequency CMOS Integrated Circuits”, Cambridge University Press, 2nd Edition, Cambridge, 2004.
2. Matthew M.Radmanesh "RF and Microwave Design Essentials”, AuthorHouse, Bloomington, 2007.
3. John W.M.Rogers and Calvin Plett, "Radio Frequency Integrated Circuit Design", 2nd Edition, Artech House, Norwood, 2010.
4. Devendra.K. Misra, "Radio Frequency and Microwave Communication Circuits – Analysis and Design”, John Wiley and Sons, Newyork, 2004.
5. Christian C. Enz Eric A. Vittoz, " Charge-based MOS Transistor Modeling - The EKV model for low-power and RF IC design", John Wiley & Sons, Ltd., 2006.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓		
CO4	✓		✓		✓	
CO5	✓		✓		✓	

NE5071 **COMPUTATIONAL INTELLIGENCE** **L T P C**
3 0 0 3

OBJECTIVES:

- To get exposed to neural network learning techniques and architectures
- To study fuzzy concepts and models
- To get exposed to hybrid neuro-fuzzy techniques
- To learn the basic concepts in Deep Learning networks
- To understand different optimization techniques and apply the same in different scenarios

UNIT - I NEURALNETWORKS **9**

Biological Neurons Networks - Artificial Neural Networks - Supervised -.unsupervised learning - Reinforcement Learning - Activation functions - Perceptrons - Back Propagation networks - Radial Basis Function Networks - Adaptive Resonance architectures - Support Vector Machines

UNIT - II FUZZY LOGIC **9**

Fuzzy Sets - Operations on Fuzzy Sets - Fuzzy Relations - Membership Functions - Fuzzy Rules and Fuzzy Reasoning - Fuzzy Inference Systems - Fuzzy Expert Systems - Fuzzy Decision Making

UNIT – III NEURO - FUZZY MODELING **9**

Adaptive Neuro - Fuzzy Inference Systems - Coactive Neuro - Fuzzy Modeling - Classification and Regression Trees - Data Clustering Algorithms - Hybrid learning algorithms - Applications of Neuro - fuzzy concepts

UNIT – IV DEEP LEARNING NETWORKS **9**

Introduction to Deep neural networks - Convolution neural networks - Deep Belief Networks - Recurrent neural networks

UNIT – V EVOLUTIONARY ALGORITHMS **9**

Heuristic search and optimization techniques -Random search - Introduction to Genetic Algorithms - Social Algorithms

TOTAL: 45 PERIODS

OUTCOMES:

On successful completion of this course, students will be able to
CO1: Design systems based on neural network architectures
CO2: Perform basic operations in fuzzy
CO3: Implement fuzzy models and work on fuzzy tool box
CO4: Design and implement deep learning architectures
CO5: Design optimization based algorithm for a given application

REFERENCES:

1. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, “Neuro - Fuzzy and Soft Computing”, Pearson Edn., 2015.
2. George J. Klir and Bo Yuan, “Fuzzy Sets and Fuzzy Logic -Theory and Applications”, Prentice Hall, 2011.
3. James A. Freeman and David M. Skapura, “Neural Networks Algorithms, Applications, and Programming Techniques”, Pearson Edn., 2003.
4. David E. Goldberg, “Genetic Algorithms in Search, Optimization and Machine Learning”, Pearson Education, 2008.
5. Ian Goodfellow, Yoshua Bengio and Aaron Courville, “Deep Learning” The MIT Press, Cambridge, 2016.

Attested

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	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓		
CO3	✓		✓	✓	✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓	✓	

VE5017 **ROBOTICS** **L T P C**
3 0 0 3

OBJECTIVES:

- To learn the fundamentals of robotics
- To learn about the dynamics of robotic controls
- To learn about the navigation mechanisms
- To learn about the hardware and software tools required for building robotic systems
- To learn about different robotic systems

UNIT - I INTRODUCTION **9**

Introduction, Rigid Transformation, Robot anatomy, Kinematics, Inverse Kinematics, Jacobians, Trajectory Following, Statics and Dynamics.

UNIT - II ARTIFICIAL LIFE AND ARTIFICIAL INTELLIGENCE **9**

History, Purpose of Robots, Artificial Intelligence, Artificial life- Nano robotics, Using neural networks in robots, Neural-Behavior based architecture, Fuzzy logic and neural sensors.

UNIT – III HARDWARE TOOLS **9**

Microcontrollers, Photovoltaic Cells, Fuel Cells, Batteries. Movement and Drive Systems- Air muscles, Nitinol wire, Solenoids, Rotary solenoids, Stepper motors, Servo Motors and DC motors. Sensors- Signal conditioning, Light sensors, Machine vision, Body sense, Direction-magnetic fields, Speech recognition, Sound and ultrasonics, Touch and Pressure, Piezoelectric material, Switches, Bend sensors, Pressure sensor, Smell, Humidity, Testing sensor.

UNIT – IV BASIC NAVIGATION **9**

Philosophies, Live Reckoning, The Best Laid Plans of Mice and Machines, Navigation as a filtering process, Hard navigation vs Fuzzy navigation, Sensors, Navigation Agents and Arbitration, Instilling pain, Fear and Confidence, Becoming unstuck in Time, Programming Robots to be useful, Command, Control and Monitoring, The Law of Conservation of Defects and the Art of Debugging.

UNIT – V DESIGN OF ROBOTS **9**

Telepresence robot, Mobile platforms, Walker Robots, Solar-ball Robot, Underwater bots, Aerobots, Robotic arm and IBM PC interface and speech control, Android hand.

TOTAL: 45 PERIODS

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OUTCOMES:

On successful completion of this course, students will be able to

CO1: Analyze the dynamics of robotics

CO2: Analyze the hardware and software requirements for robotics

CO3: Build a miniature robotic system

CO4: Design of navigation mechanisms involved in building a robotic system

CO5: To be able to know about different robotic systems

REFERENCES:

1. J. M. Selig, "Introductory Robotics", Prentice Hall, 1992.
2. John Iovine, "Robots, Android and Animatronics", Second Edition, McGraw-Hill, 2002.
3. John M. Holland, "Designing Autonomous Mobile Robots-Inside the mind of an Intelligent Machine", Newnes Publication, 2004.
4. Robert J. Schiling, "Fundamentals of Robotics- Analysis and Control", Pearson Education, 2006.
5. Bruno Siciliano, Lorenzo Sciavicco, Luigi Villani and Giuseppe Oriolo, "Robotics- Modelling, Planning and Control", Springer-Verlag London Limited 2010.

	PO1	PO2	PO3	PO4	PO5	PO6
CO1	✓		✓	✓		✓
CO2	✓		✓	✓	✓	
CO3	✓		✓	✓	✓	
CO4	✓		✓		✓	
CO5	✓		✓	✓	✓	

OE5091 **BUSINESS DATA ANALYTICS** **L T P C**

3 0 0 3

OBJECTIVES:

- To understand the basics of business analytics and its life cycle.
- To gain knowledge about fundamental business analytics.
- To learn modeling for uncertainty and statistical inference.
- To understand analytics using Hadoop and Map Reduce frameworks.
- To acquire insight on other analytical frameworks.

UNIT I OVERVIEW OF BUSINESS ANALYTICS **9**

Introduction – Drivers for Business Analytics – Applications of Business Analytics: Marketing and Sales, Human Resource, Healthcare, Product Design, Service Design, Customer Service and Support – Skills Required for a Business Analyst – Framework for Business Analytics Life Cycle for Business Analytics Process.

Suggested Activities:

- Case studies on applications involving business analytics.
- Converting real time decision making problems into hypothesis.
- Group discussion on entrepreneurial opportunities in Business Analytics.

Suggested Evaluation Methods:

- Assignment on business scenario and business analytical life cycle process.
- Group presentation on big data applications with societal need.
- Quiz on case studies.

UNIT II ESSENTIALS OF BUSINESS ANALYTICS 9

Descriptive Statistics – Using Data – Types of Data – Data Distribution Metrics: Frequency, Mean, Median, Mode, Range, Variance, Standard Deviation, Percentile, Quartile, z-Score, Covariance, Correlation – Data Visualization: Tables, Charts, Line Charts, Bar and Column Chart, Bubble Chart, Heat Map – Data Dashboards.

Suggested Activities:

- Solve numerical problems on basic statistics.
- Explore chart wizard in MS Excel Case using sample real time data for data visualization.
- Use R tool for data visualization.

Suggested Evaluation Methods:

- Assignment on descriptive analytics using benchmark data.
- Quiz on data visualization for univariate, bivariate data.

UNIT III MODELING UNCERTAINTY AND STATISTICAL INFERENCE 9

Modeling Uncertainty: Events and Probabilities – Conditional Probability – Random Variables – Discrete Probability Distributions – Continuous Probability Distribution – Statistical Inference: Data Sampling – Selecting a Sample – Point Estimation – Sampling Distributions – Interval Estimation – Hypothesis Testing.

Suggested Activities:

- Solving numerical problems in sampling, probability, probability distributions and hypothesis testing.
- Converting real time decision making problems into hypothesis.

Suggested Evaluation Methods:

- Assignments on hypothesis testing.
- Group presentation on real time applications involving data sampling and hypothesis testing.
- Quizzes on topics like sampling and probability.

UNIT IV ANALYTICS USING HADOOP AND MAPREDUCE FRAMEWORK 9

Introducing Hadoop – RDBMS versus Hadoop – Hadoop Overview – HDFS (Hadoop Distributed File System) – Processing Data with Hadoop – Introduction to MapReduce – Features of MapReduce – Algorithms Using Map-Reduce: Matrix-Vector Multiplication, Relational Algebra Operations, Grouping and Aggregation – Extensions to MapReduce.

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Suggested Activities:

- Practical – Install and configure Hadoop.
- Practical – Use web based tools to monitor Hadoop setup.
- Practical – Design and develop MapReduce tasks for word count, searching involving text corpus etc.

Suggested Evaluation Methods:

- Evaluation of the practical implementations.
- Quizzes on topics like HDFS and extensions to MapReduce.

UNIT V OTHER DATA ANALYTICAL FRAMEWORKS 9

Overview of Application development Languages for Hadoop – PigLatin – Hive – Hive Query Language (HQL) – Introduction to Pentaho, JAQL – Introduction to Apache: Sqoop, Drill and Spark, Cloudera Impala – Introduction to NoSQL Databases – Hbase and MongoDB.

Suggested Activities:

- Practical – Installation of NoSQL database like MongoDB.
- Practical – Demonstration on Sharding in MongoDB.
- Practical – Install and run Pig
- Practical – Write PigLatin scripts to sort, group, join, project, and filter data.
- Design and develop algorithms to be executed in MapReduce involving numerical methods for analytics.

Suggested Evaluation Methods:

- Mini Project (Group) – Real time data collection, saving in NoSQL, implement analytical techniques using Map-Reduce Tasks and Result Projection.

TOTAL: 45 PERIODS

OUTCOMES:

On completion of the course, the student will be able to:

- Identify the real world business problems and model with analytical solutions.
- Solve analytical problem with relevant mathematics background knowledge.
- Convert any real world decision making problem to hypothesis and apply suitable statistical testing.
- Write and Demonstrate simple applications involving analytics using Hadoop and MapReduce
- Use open source frameworks for modeling and storing data.
- Apply suitable visualization technique using R for visualizing voluminous data.

REFERENCES:

1. Vignesh Prajapati, “Big Data Analytics with R and Hadoop”, Packt Publishing, 2013.
2. Umesh R Hodeghatta, Umesha Nayak, “Business Analytics Using R – A Practical Approach”, Apress, 2017.
3. Anand Rajaraman, Jeffrey David Ullman, “Mining of Massive Datasets”, Cambridge University Press, 2012.
4. Jeffrey D. Camm, James J. Cochran, Michael J. Fry, Jeffrey W. Ohlmann, David R. Anderson, “Essentials of Business Analytics”, Cengage Learning, second Edition, 2016.
5. U. Dinesh Kumar, “Business Analytics: The Science of Data-Driven Decision Making”, Wiley, 2017.
6. A. Ohri, “R for Business Analytics”, Springer, 2012
7. Rui Miguel Forte, “Mastering Predictive Analytics with R”, Packt Publication, 2015.

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	PO1	PO2	PO3	PO4	PO5	PO6
CO1	1	1	1	2	3	1
CO2	2	1	1	2	1	1
CO3	1	1	2	3	3	1
CO4	2	2	1	2	1	1
CO5	1	1	2	2	1	1
CO6	1	1	1	3	2	1

OE5092 **INDUSTRIAL SAFETY** **L T P C**
3 0 0 3

OBJECTIVES:

- Summarize basics of industrial safety
- Describe fundamentals of maintenance engineering
- Explain wear and corrosion
- Illustrate fault tracing
- Identify preventive and periodic maintenance

UNIT I INTRODUCTION **9**

Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II FUNDAMENTALS OF MAINTENANCE ENGINEERING **9**

Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III WEAR AND CORROSION AND THEIR PREVENTION **9**

Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV FAULT TRACING **9**

Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

Attested

UNIT V PERIODIC AND PREVENTIVE MAINTENANCE 9

Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able to:

CO1: Ability to summarize basics of industrial safety

CO2: Ability to describe fundamentals of maintenance engineering

CO3: Ability to explain wear and corrosion

CO4: Ability to illustrate fault tracing

CO5: Ability to identify preventive and periodic maintenance

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES:

1. Audels, Pump-hydraulic Compressors, Mcgrew Hill Publication, 1978.
2. Garg H P,Maintenance Engineering, S. Chand and Company,1987.
3. Hans F. Winterkorn, Foundation Engineering Handbook, Chapman & Hall London, 2013.
4. Higgins & Morrow, Maintenance Engineering Handbook, Eighth Edition,2008

OE5093 OPERATIONS RESEARCH L T P C

3 0 0 3

OBJECTIVES:

- Solve linear programming problem and solve using graphical method.
- Solve LPP using simplex method
- Solve transportation, assignment problems
- Solve project management problems
- Solve scheduling problems

UNIT I LINEAR PROGRAMMING 9

Introduction to Operations Research – assumptions of linear programming problems – Formulations of linear programming problem – Graphical method

UNIT II ADVANCES IN LINEAR PROGRAMMING 9

Solutions to LPP using simplex algorithm- Revised simplex method - primal dual relationships – Dual simplex algorithm - Sensitivity analysis

UNIT III NETWORK ANALYSIS – I 9

Transportation problems -Northwest corner rule, least cost method, Voges's approximation method - Assignment problem -Hungarian algorithm

UNIT IV NETWORK ANALYSIS – II 9

Shortest path problem: Dijkstra's algorithms, Floyds algorithm, systematic method -CPM/PERT

UNIT V NETWORK ANALYSIS – III 9

Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able to:

CO1: To formulate linear programming problem and solve using graphical method.

CO2: To solve LPP using simplex method

CO3: To formulate and solve transportation, assignment problems

CO4: To solve project management problems

CO5: To solve scheduling problems

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES:

1. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010
2. Hitler Libermann, Operations Research: McGraw Hill Pub. 2009
3. Pant J C, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008
4. Pannerselvam, Operations Research: Prentice Hall of India 2010
5. Taha H A, Operations Research, An Introduction, PHI, 2008

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OE5094 COST MANAGEMENT OF ENGINEERING PROJECTS

L T P C
3 0 0 3

OBJECTIVES:

- Summarize the costing concepts and their role in decision making
- Infer the project management concepts and their various aspects in selection
- Interpret costing concepts with project execution
- Develop knowledge of costing techniques in service sector and various budgetary control techniques
- Illustrate with quantitative techniques in cost management

UNIT I INTRODUCTION TO COSTING CONCEPTS 9

Objectives of a Costing System; Cost concepts in decision-making; Relevant cost, Differential cost, Incremental cost and Opportunity cost; Creation of a Database for operational control.

UNIT II INTRODUCTION TO PROJECT MANAGEMENT 9

Project: meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities, Detailed Engineering activities, Pre project execution main clearances and documents, Project team: Role of each member,Importance Project site: Data required with significance, Project contracts.

UNIT III PROJECT EXECUTION AND COSTING CONCEPTS 9

Project execution Project cost control, Bar charts and Network diagram, Project commissioning: mechanical and process, Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis, Various decision-making problems, Pricing strategies: Pareto Analysis, Target costing, Life Cycle Costing.

UNIT IV COSTING OF SERVICE SECTOR AND BUDGETERY CONTROL 9

Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis, Budgetary Control: Flexible Budgets; Performance budgets; Zero-based budgets.

UNIT V QUANTITATIVE TECHNIQUES FOR COST MANAGEMENT 9

Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Learning Curve Theory.

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able to:

CO1 – Understand the costing concepts and their role in decision making

CO2–Understand the project management concepts and their various aspects in selection

CO3–Interpret costing concepts with project execution

CO4–Gain knowledge of costing techniques in service sector and various budgetary control techniques

CO5 - Become familiar with quantitative techniques in cost management

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	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓	✓	✓		✓			✓	✓		✓	✓
CO2	✓	✓	✓		✓				✓		✓	✓
CO3	✓	✓	✓		✓	✓					✓	✓
CO4	✓	✓	✓		✓		✓				✓	✓
CO5	✓	✓	✓		✓	✓	✓				✓	✓

REFERENCES:

1.Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher, 1991
2. Charles T. Horngren and George Foster, Advanced Management Accounting, 1988
3. Charles T. Horngren et al Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi, 2011
4. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting, 2003
5. Vohra N.D., Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd, 2007

OE5095 COMPOSITE MATERIALS L T P C
3 0 0 3

OBJECTIVES:

- Summarize the characteristics of composite materials and effect of reinforcement in composite materials.
- Identify the various reinforcements used in composite materials.
- Compare the manufacturing process of metal matrix composites.
- Understand the manufacturing processes of polymer matrix composites.
- Analyze the strength of composite materials.

UNIT I INTRODUCTION 9

Definition – Classification and characteristics of Composite materials - Advantages and application of composites - Functional requirements of reinforcement and matrix - Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT II REINFORCEMENTS 9

Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers - Properties and applications of whiskers, particle reinforcements - Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures - Isostrain and Isostress conditions.

UNIT III MANUFACTURING OF METAL MATRIX COMPOSITES 9

Casting – Solid State diffusion technique - Cladding – Hot isostatic pressing - Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving - Properties and applications.

UNIT IV MANUFACTURING OF POLYMER MATRIX COMPOSITES 9

Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding - Properties and applications.

UNIT V STRENGTH **9**

Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able to:

- CO1 - Know the characteristics of composite materials and effect of reinforcement in composite materials.
- CO2 – Know the various reinforcements used in composite materials.
- CO3 – Understand the manufacturing processes of metal matrix composites.
- CO4 – Understand the manufacturing processes of polymer matrix composites.
- CO5 – Analyze the strength of composite materials.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1		✓	✓	✓								
CO2		✓	✓	✓	✓						✓	
CO3			✓	✓	✓		✓				✓	
CO4			✓	✓	✓		✓				✓	
CO5			✓	✓	✓		✓					

REFERENCES:

1. Cahn R.W. - Material Science and Technology – Vol 13 – Composites, VCH, West Germany.
2. Callister, W.D Jr., Adapted by Balasubramaniam R, Materials Science and Engineering, An introduction, John Wiley & Sons, NY, Indian edition, 2007.
3. Chawla K.K., Composite Materials, 2013.
4. Lubin.G, Hand Book of Composite Materials, 2013.

OE5096 **WASTE TO ENERGY** **L T P C**
3 0 0 3

OBJECTIVES:

- Interpret the various types of wastes from which energy can be generated
- Develop knowledge on biomass pyrolysis process and its applications
- Develop knowledge on various types of biomass gasifiers and their operations
- Invent knowledge on biomass combustors and its applications on generating energy
- Summarize the principles of bio-energy systems and their features

UNIT I INTRODUCTION TO EXTRACTION OF ENERGY FROM WASTE **9**

Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT II BIOMASS PYROLYSIS **9**

Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III BIOMASS GASIFICATION 9

Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV BIOMASS COMBUSTION 9

Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V BIO ENERGY 9

Properties of biogas (Calorific value and composition), Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production -Urban waste to energy conversion - Biomass energy programme in India.

TOTAL: 45 PERIODS

OUTCOMES:

Students will be able to:

CO1 – Understand the various types of wastes from which energy can be generated

CO2 – Gain knowledge on biomass pyrolysis process and its applications

CO3 – Develop knowledge on various types of biomass gasifiers and their operations

CO4 – Gain knowledge on biomass combustors and its applications on generating energy

CO5 – Understand the principles of bio-energy systems and their features

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓		✓									✓
CO2	✓		✓									✓
CO3	✓	✓	✓		✓							✓
CO4	✓	✓	✓		✓		✓					✓
CO5	✓	✓	✓		✓							✓

REFERENCES:

1. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.

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AUDIT COURSES (AC)

AX5091 ENGLISH FOR RESEARCH PAPER WRITING L T P C
2 0 0 0

OBJECTIVES

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING 6

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS 6

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first-time submission

TOTAL: 30 PERIODS

OUTCOMES

CO1 –Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1										✓		✓
CO2										✓		✓
CO3										✓		✓
CO4										✓		✓
CO5										✓		✓

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REFERENCES

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX5092 DISASTER MANAGEMENT L T P C
2 0 0 0

OBJECTIVES

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

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OUTCOMES

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO5: Ability to develop the strengths and weaknesses of disaster management approaches

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	✓											
CO2	✓											
CO3	✓	✓	✓									
CO4	✓	✓	✓									
CO5	✓	✓	✓									

REFERENCES

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX5093 SANSKRIT FOR TECHNICAL KNOWLEDGE L T P C
2 0 0 0

OBJECTIVES

- Illustrate the basic sanskrit language.
- Recognize sanskrit, the scientific language in the world.
- Appraise learning of sanskrit to improve brain functioning.
- Relate sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- Extract huge knowledge from ancient literature.

UNIT I ALPHABETS **6**

Alphabets in Sanskrit

UNIT II TENSES AND SENTENCES **6**

Past/Present/Future Tense - Simple Sentences

UNIT III ORDER AND ROOTS **6**

Order - Introduction of roots

UNIT IV SANSKRIT LITERATURE **6**

Technical information about Sanskrit Literature

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UNIT V TECHNICAL CONCEPTS OF ENGINEERING 6

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TOTAL: 30 PERIODS

OUTCOMES

- CO1 - Understanding basic Sanskrit language.
- CO2 - Write sentences.
- CO3 - Know the order and roots of Sanskrit.
- CO4 - Know about technical information about Sanskrit literature.
- CO5 - Understand the technical concepts of Engineering.

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1										✓		✓
CO2										✓		✓
CO3												✓
CO4												✓
CO5												✓

REFERENCES

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi, 2017.

AX5094 VALUE EDUCATION L T P C

2 0 0 0

OBJECTIVES

Students will be able to

- Understand value of education and self-development
- Imbibe good values in students
- Let the should know about the importance of character

UNIT I

Values and self-development–Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non-moral valuation. Standards and principles. Value judgements

UNIT II

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT III

Personality and Behavior Development-Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brother hood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT IV

Character and Competence–Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

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TOTAL: 30 PERIODS

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OUTCOMES

Students will be able to

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

SUGGESTED READING

1. Chakroborty, S.K."Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

AX5095	CONSTITUTION OF INDIA	L	T	P	C
		2	0	0	0

OBJECTIVES

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION:

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION:

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES:

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE:

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION:

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION:

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

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OUTCOMES

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX5096 PEDAGOGY STUDIES L T P C
2 0 0 0

OBJECTIVES

Students will be able to:

- Review existing evidence on there view topic to inform programme design and policy
- Making under taken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

UNIT I INTRODUCTION AND METHODOLOGY:

Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions **-** Overview of methodology and Searching.

UNIT II THEMATIC OVERVIEW

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES

Methodology for the in depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV PROFESSIONAL DEVELOPMENT

Professional development: alignment with classroom practices and follow up support - Peer support - Support from the head teacher and the community - Curriculum and assessment - Barriers to learning: limited resources and large class sizes

UNIT V RESEARCH GAPS AND FUTURE DIRECTIONS

Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment - Dissemination and research impact.

TOTAL: 30 PERIODS

OUTCOMES

Students will be able to understand:

- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

SUGGESTED READING

1. Ackers J, HardmanF (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245-261.
2. Agrawal M (2004)Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36(3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana-does it count? Multi-site teacher education research project (MUSTER) country report 1.London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33(3): 272–282.
5. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M(2003) Read India: Amass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf

AX5097 STRESS MANAGEMENT BY YOGA L T P C
2 0 0 0

OBJECTIVES

- To achieve overall health of body and mind
- To overcome stress

UNIT I

Definitions of Eight parts of yoga.(Ashtanga)

UNIT II

Yam and Niyam - Do`s and Don't's in life - i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Ahinsa, satya, astheya, bramhacharya and aparigraha.

UNIT III

Asan and Pranayam - Various yog poses and their benefits for mind & body - Regularization of breathing techniques and its effects-Types of pranayam

TOTAL: 30 PERIODS

OUTCOMES

Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

SUGGESTED READING

1. 'Yogic Asanas for Group Tarining-Part-I":Janardan Swami Yoga bhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

AX5098	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	L T P C 2 0 0 0

OBJECTIVES

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

UNIT I

Neetisatakam-holistic development of personality - Verses- 19,20,21,22 (wisdom) - Verses- 29,31,32 (pride & heroism) – Verses- 26,28,63,65 (virtue) - Verses- 52,53,59 (dont's) - Verses- 71,73,75,78 (do's)

UNIT II

Approach to day to day work and duties - Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48 - Chapter 3-Verses 13, 21, 27, 35 Chapter 6-Verses 5,13,17,23, 35 - Chapter 18-Verses 45, 46, 48.

UNIT III

Statements of basic knowledge - Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 - Verses 13, 14, 15, 16,17, 18 - Personality of role model - shrimad bhagwad geeta - Chapter2-Verses 17, Chapter 3-Verses 36,37,42 - Chapter 4-Verses 18, 38,39 Chapter18 – Verses 37,38,63

TOTAL: 30 PERIODS

OUTCOMES

Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neet is hatakam will help in developing versatile personality of students.

SUGGESTED READING

1. Gopinath, Rashtriya Sanskrit Sansthanam P, Bhartrihari's Three Satakam, Niti-sringar-vairagya, New Delhi,2010
2. Swami Swarupananda , Srimad Bhagavad Gita, Advaita Ashram, Publication Department, Kolkata, 2016.

Attested

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